IJRSET March 2016 Volume 3, Issue 3 Pages: 57-62
ISSN 2394-739X
International Journal for Research in Science Engineering and Technology

DESIGN AND IMPLEMENTATION OF ERSFQ BASED GDI TECHNIQUE USING TANNER

[1] G. Abirami, [2] Punithavathy Mohan M.E.,(Ph.D),
[1] M.Tech Department of ECE, [2] Professor, Department of ECE,
[1, 2] Hindustan University,
[1, 2] Padur, Tamilnadu,
[1, 2] India.

Abstract:-

Rapid Single Flux Quantum (RSFQ) is a digital electronic technology that uses superconducting devices to process the digital signals. The information is stored in the form of magnetic flux quanta, in RFSQ logic. Resistor-free approach to dc biasing of RSFQ logical circuits are known as Energy-efficient Rapid Single Flux Quantum (ERSFQ) that does not use bias resistors. The ERSFQ logic is to eliminate the static power loss of RSFQ by replacing bias resistors with set of inductors and current-limiting Josephson junction. Traditionally, the ERSFQ logical circuit is designed in this paper. In the ERSFQ architecture, numbers of half adders are used to design this structure. The main disadvantage of ERFSQ structure, the number of transistor count is increased. In order to reduce this problem, ERFSQ based GDI (Gate Diffusion Input) technique is proposed in this paper. The schematic circuit of proposed ERSFQ based GDI technique is designed by using Tanner EDA tool.

Keywords: - Rapid Single Flux Quantum (RSFQ), Energy-efficient Rapid Single Flux Quantum (ERSFQ), Electronic Design Automation (EDA).

1. INTRODUCTION

In 1987, the problem of static power dissipation in Rapid Single-Flux-Quantum (RSFQ) has been discussed and it was invented by K.Likharev.RSFQ logic circuits the signals are passed in the form of short pulses. These logic circuits employ a new concept of digitizing, which is used to utilize quantum properties of Josephson circuits and make faster circuits. The maturity of RSFQ technology, get rid of static and reducing total power dissipation has become a very important problem. RSFQ LSI systems require sharp reduction in power dissipation. In the circuit, static power dissipation is called as “Ideal breaker”, so many of the researchers have applied these efforts to solve the problem.

The circuit density and the energy-efficiency of the CMOS integrated circuits have been increased by scaling down their physical sizes using the cutting –edge fabrication processes in [K.Inoue, 2013]. Cryocooler-based RSFQ LSI systems need sharp reduction in power dissipation. The practical idea was to reduce value of bias resistors. The working of RSFQ circuit creates dc voltage drops between its parts equal to or less than ΔV [D.E.Kirichenko, 2010]. In [Andrea M. Herr] the RSFQ recurrent circuit is the circular shift register

(CSR). The RSFQ digital signal processing circuit is an oversampling analog-to-digital converter with an 18-bit decimation filter consists of 2100 Josephson junction operating above 10-GHz clock frequency.

The attractive properties of RSFQ logic is local timing. RSFQ propagate together with data in the clock pulses, it suitable for high-speed architecture. The maximum operating speed of the static frequency divider depends on the toggle flip-flop gate. This method does not allow to calculating the yield of a fabrication process due to simplicity of TFF. Gate Diffusion Input (GDI) technique helps in designing low-power digital combinational circuit. GDI technique allows reducing power consumption, propagation delay and area of digital circuits. GDI technique is suitable for the design of fast and low power circuits using reduced number of transistors in CMOS and PTL techniques.

In this paper, the proposed ERSFQ based GDI technique is designed to reduce the area, delay and power consumption. The schematic circuit of ERSFQ based GDI technique is used to improve the performances of the architecture and also reduces the number of transistor counts.

2. LITERATURE REVIEW

Optimized power consumption in superconducting electronics has been described in [Thomas ortlepp, et al, 2011].RSFQ design has a large potential for reducing the power consumption in operation stability. The two potential techniques of this reduction consists of reduced critical current and reduced supply voltages. The different approaches for the static power consumption is reduced by searching the potential of inductive bias distribution networks. The system design of RSFQ circuits is the interface cells between RSFQ and semiconductor electronics.

High –speed operation of a 64-bit circular shift register (CSR) has been explained in [Andrea M.Herr, et al, 1998]. The CSR is an important RSFQ circuit with many applications. CSR's can be used as serial memory in digital signal processors which need data to be repeatedly accessed such as coefficients of a digital filter.With the addition of XOR gate the CSR becomes Pseudo-random number generator.

Delay insensitive RSFQ circuits with zero static power dissipation have been described in [Stas polonsky, 1999]. Delay Insensitive (DI) RSFQ primitives can be modified so that resistors are not needed in the dc power supply distribution network, and also the on-chip static power dissipation is absent. RSFQ circuits to avoid using resistive bias resistor for complex parallel circuits. RSFQ primitives can be modified to allow purely inductive power distribution networks with zero static power dissipation.

Zero static power dissipation biasing of RSFQ circuits has been explained in [D.E. Kirichenko, 2011]. The RSFQ circuits provide zero static and minimal total power dissipation.ERSFQ circuits at low frequency containing D flip-flop with complementary outputs and two static frequency dividers. ERSFQ biasing scheme does not dissipate energy in the static mode and dissipates orders of magnitude less power.

3. ENERGY- EFFICIENT RAPID SINGLE FLUX QUANTUM (ERSFQ) 8-BIT WAVE PIPELINE ADDER

ERSFQ is the absolute compatibility with RSFQ, that the RSFQ circuit can be easily converted to ERSFQ by attaching a feeding Josephson Transmission Line (JTL) to the bias line and simple substitution of bias resistors. The fragment of an ERSFQ circuit is designed for the standard HYPRES 4.5KA/cm^2 process. The bias inductors consuming substantial space on a chip. The bias inductances are not restricted in value; it can be moved to any place on a chip. The working on these inductances are moved under the ground plane by adding an some

extra superconductor layer to the process. This layer is made up of superconductor with a high kinetic inductance. The drawback of ERSFQ is high time jitter due to unavoidable bias current fluctuations $\delta I \leq \Phi_0/L_b$. The solution is to increasing value L_b of a bias inductor and generally employing pipeline architecture in large circuits. The Layout fragment of ERSFQ circuit is illustrated in fig. 1. The fabricated ERSFQ circuit is to obtain large inductance, ground planes were removed from under the inductor.

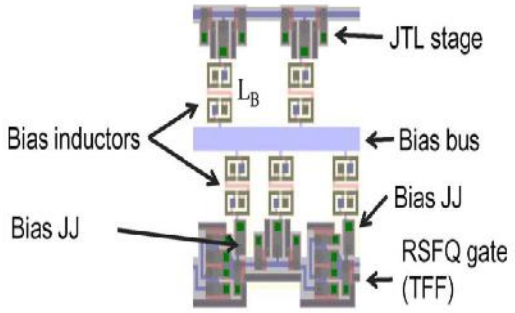

Figure.1 Layout Fragment of ERSFQ Circuit

ERSFQ approach has designed two version of an 8-bit parallel adder wave – pipelined architecture. The schematic architecture of the 8-bit wave pipelined adder is illustrated in fig. 2. The adders were designed with an asynchronous carry half-adder (HA) cell. This half adder cell comprises a hybrid between an asynchronous C element and B flip-flop. It is insensitive to the delay elements between the inputs and allowing high throughput operation of the adder. The design of fig 2 was a most straight-forward approach imposed by the aligned data front requirement. To avoid using merge cell in ERSFQ design.

In this architecture, clock signal follows the data in a single-clock operation. The half adder cells are needed clock for producing the SUM (XOR) output, while the CARRY (AND) output signal is being generated and propagated asynchronously. The main drawback of this design is its large size and also the number of transistor count is increased. In order to reduce this problem, the ERSFQ based GDI technique is proposed.

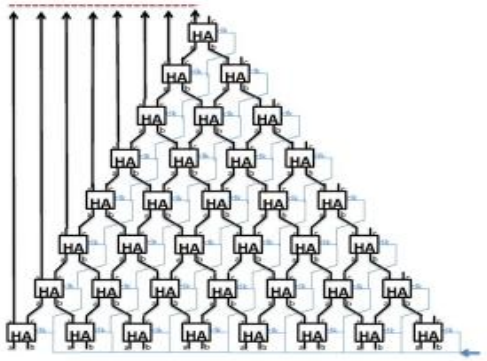

Figure. 2 Schematic of the "aligned-front" 8-bit wave pipeline adder

4. PROPOSED ENERGY-EFFICIENT RAPID SINGLE FLUX QUANTUM (ERSFQ) BASED GATE DIFFUSION INPUT (GDI) TECHNIQUE

In this paper, the proposed Energy-efficient Rapid Single Flux Quantum (ERSFQ) based Gate Diffusion Input (GDI) technique has been designed. The GDI technique which is used to reducing power consumption, latency and area of digital circuits. Traditionally, ERSFQ based CMOS design of AND gate and XOR gate are increased in the number of transistor counts. To avoid this problem, proposed design of ERSFQ based GDI technique which is used to reduce the number of transistor counts in AND gate and XOR gate. The GDI basic cell is shown in figure 3.

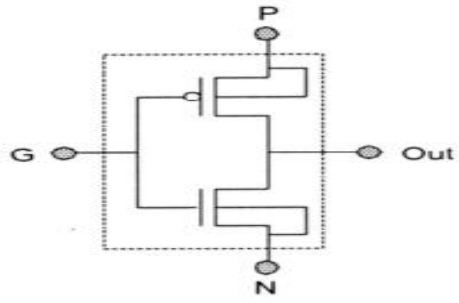

Figure.3 GDI basic cells

In the traditional method of ERSFQ based CMOS design of XOR gate, the number of transistor count is 12. And, ERSFQ based CMOS design of AND gate, the number of transistor count is 6. In the proposed method of ERSFQ based GDI technique of XOR gate and AND gate , the reduced number of transistor count is 4 and 2. The CMOS design of XOR gate is illustrated in fig.4 and also the GDI designof XOR gate is illustrated in fig. 5. The CMOS design of XOR gate is shown in fig.6 and the GDI design of AND gate is shown in fig.7. ERSFQ based GDI technique, which is used to improve the performances of the structure. The schematic design of XOR and AND gate is shown in fig.8 and fig.9.

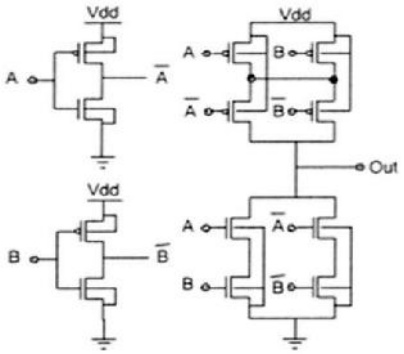

Figure. 4 CMOS design of XOR gate

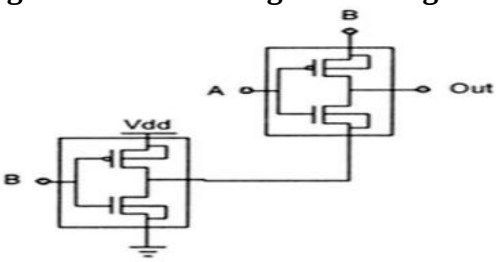

Figure.5 GDI design of XOR gate

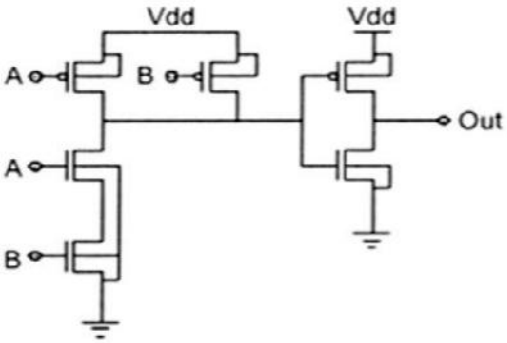

Figure.6 CMOS design of AND gate

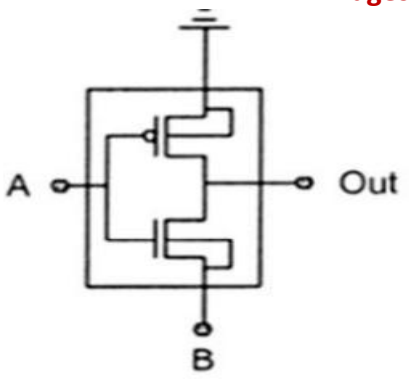

Figure.7 GDI design of AND gate

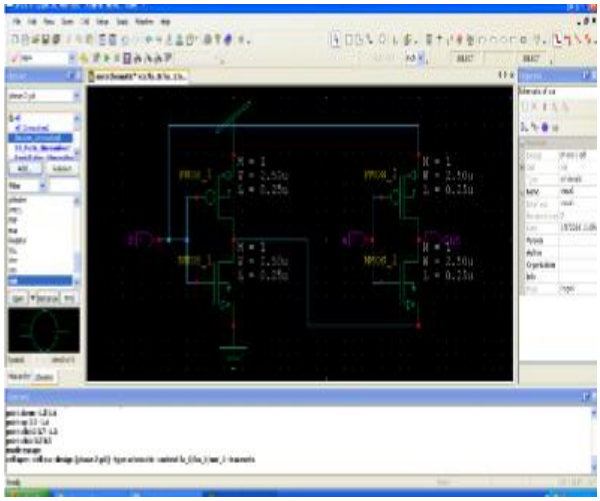

Figure.8 Schematic design of AND gate using GDI technique

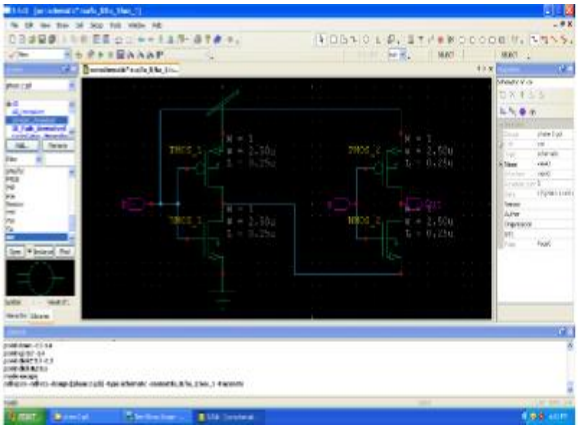

Figure. 9 Schematic design of XOR gate using GDI technique

5. RESULTS AND DISCUSSION

The schematic design of ERSFQ based GDI technique is designed through Back End Tanner Electronic Design Automation (EDA) v14.1i tool. In this paper, ERSFQ based GDI is used to reduce

the number of transistor counts. The schematic RTL view of 8-bit wave pipeline adder is shown in fig.10.

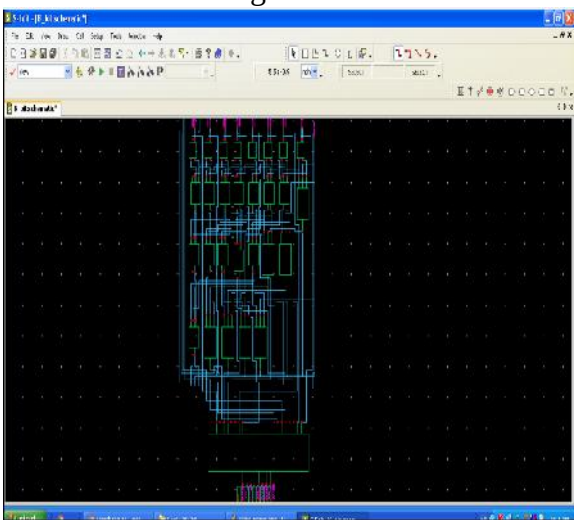

Figure.10 Schematic RTL view of 8-bit wave pipeline adder

The synthesis result of area and power as shown in fig 11 and fig 12. The proposed ERSFQ based GDI technique , the power value is 12mv. The device and node counts of MOSFETs are 216, voltage sources are16, MOSFET geometrics are 2, and Subcircuit instances are 108.

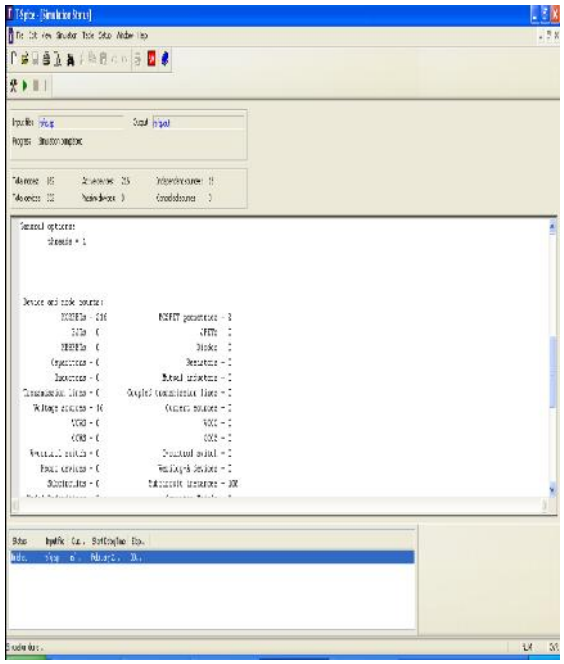

Figure 11. Synthesis result of area for ERSFQ based GDI .

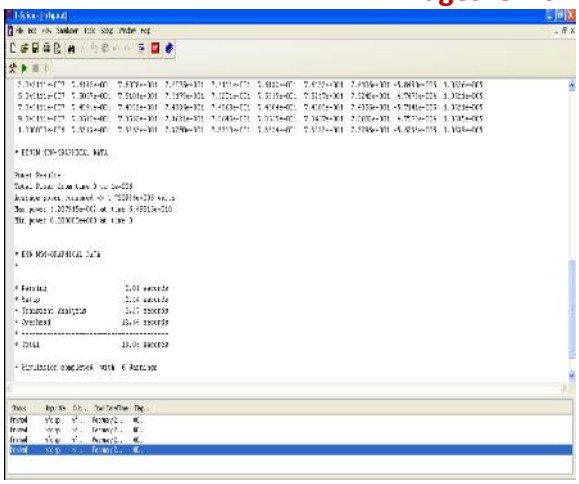

Figure 12. Synthesis result of power for ERSFQ based GDI.

CONCLUSION

In this paper, Energy-Efficient Rapid Single Flux Quantum (ERSFQ) based GDI technique is designed using Tanner through Very Large Scale Integration (VLSI) System design environment. Less area utilization, high speed and lower power consumption are the main key factors in VLSI system design environment. Therefore, the main aim of this paper is to reduce the number of transistor counts and power consumption. Finally, ERSFQ based GDI techniques are proposed in this paper. The power is 12mv in ERSFQ based GDI technique. When compared to ERSFQ based CMOS design, ERSFQ based GDI gives better performance.

REFERENCES

[1]. Rylyakov and K. K. Likharev, “Pulse jitter and timing errors in RSFQ circuits,”IEEE Trans. Appl. Supercond., vol. 9, no. 2, pp. 3539–3444, Jun. 1999.

[2]. D. S. Holmes, A. L. Ripple, and M. A. Manheimer, “Energy-efficient superconducting computing—Power budgets and requirements,” IEEE Trans. Appl. Supercond., vol. 23, no. 3, Jun. 2013, Art. ID. 1701610.

[3]. V. Vernik et al., “Progress in the development of cryocooled digital channelizing RF receivers,”IEEE Trans.

Appl. Supercond., vol. 19, no. 3,pp. 1016–1021, Jun. 2009.
[4]. K. K. Likharev and V. K. Semenov, “RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz clock-frequency digital systems,” IEEE Trans. Appl. Supercond., vol. 1, no. 1, pp. 3–28,Mar. 1991.
[5]. M. D. Niemacket al., “Code-division SQUID multiplexing,” Appl. Phys.Lett., vol. 96, no. 16, Apr 2010, Art. ID. 163509.
[6]. M. Steffen, D. P. DiVincenzo, J. M. Chow, T. N. Theis, and M. B. Ketchen, “Quantum computing: An IBM perspective,”IBM J. Res.Develop., vol. 55, no. 5, pp. 13:1–13:11, Sep./Oct. 2011.
[7]. O. A. Mukhanov et al., “Superconductor digital-RF receiver systems,” IEICE Trans. Electron., vol. E91-C, no. 3, pp. 306–317, Mar. 2008.
[8]. R. F. Service, “What it’ll take to go to exascale,” Science, vol. 335,no. 6067, pp. 394–396, Jan. 2012.
[9]. S. Borkar and A. Chien, “The future of microprocessors,”Commun. ACM,vol. 54, no. 5, pp. 67–77, May 2011.
[10]. S. Mikiet al., “Superconducting single photon detectors integrated with single flux quantum readout circuits in a cryocooler,”Appl. Phys. Lett.vol. 99, no. 11, Sep. 2011, Art. ID. 111108.