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DESIGN OF RELIABLE NETWORK ON CHIP (NOC) ROUTER BASED PACKET SWITCHING METHOD

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Abstract:-

Network- on- Chip (NOC) has developed as a new model to integrate large number of cores on a single silicon die. The NOC architecture is the on-chip communication infrastructure consist of physical layer, the data link layer and the network layer of OSI protocol stack. In this paper, NOC router based packet switching network with Round Robin Arbiter is proposed. In packet switching method, data's are transmitted in short packets. Packets are received, stored briefly and forward to the next node. The packet switching network with virtual channel flow control provides the flexibility, area and energy efficiency and also . All packets are routed through the shortest paths and maintaining the performance of Noc in the presence of faults. The main goal of this work is to reduce the frequent checking of unconnected nodes and making the return path delay. In this proposed design, is to reduce the power, delay and area and also improves the performance of the architecture. NoC data transport medium is occupied by routers, which is predominantly occupied by FIFO buffers and routing logic. Arbiter is used in network on chip when number of input are requested for same output port , the arbiter has produce the signal on the basis of that number of input port getting a priority and the input port transmit a packet to output port.

Keywords: - Network on Chip (NOC), First –In –First -Out (FIFO).

1. INTRODUCTION

With the increasing large number of cores in a single chip, on-chip communication efficiency has become one of the important key factors calculating overall system performance and cost. System on a chip (SoC) is the design technique currently used by VLSI designers, established on extensive IP core reuse. Dedicated wires are effective only for systems with a limited number of cores, since the number of wires in the system upgrades dramatically as the number of cores grows. Therefore, dedicated wires have poor reusability and flexibility. Significant amount of area of the NoC data transport medium is employed by routers, which is predominantly employed by FIFO

buffers and routing logic. Accordingly, the probabilities of run-time faults occurring in buffers and logic are drastically higher compared with the other components of the NoC. Thus, NoC infrastructure of test process must begin with test of buffers and routing logic of the routers. In addition, the test must be implemented periodically to ensure that no fault gets accumulated. By using short messages, packet switching is similar to message switching .Any message exceeding a network-defined maximum length is damaged up into shorter units, known as packets .For transmission the packets, each with an associated header, are transmitted individually through the network. The Packet Switching performance is called Best Effort performance. If transmit from sender to receiver, the entire network will do its best to get the packet to the other end as fast as possible, but there are no guarantees on how fast that packet will arrive. A network on chip (NoC) appears as a probable better solution to perform future on-chip interconnection architectures. In the most commonly found organization, a NoC is a regular of attached switches, with IP cores attached to these switches. NoCs present better performance, bandwidth, and scalability than shared busses. Switches are responsible for: (a) receiving incoming packets; (b) storing packets; (c) routing these packets to a given output port; (d) sending packets to others switches. In this paper, the proposed NoC based packet switching network with round robin arbiter is designed. This method is used to collect all the direction of information signal in a single direction and transfer that information from one source to another destination. Packet switching is the most employed switching mechanism in NoCs, although circuit switching NoCs have been proposed. Packet switching desires the use of a switching mode, which specify how packets move through the switches. Round robin arbiter is reduce the time spent on arbiter design.

2. LITERATURE REVIEW

[Younes M. Boura, et al] have proposed an Efficient fully adaptive wormhole routing in n-dimensional Meshes.The routing algorithm provides full adaptively at a cost of single additional virtual channel per physical channel irrespective to the number of dimensions of the network. The algorithm is based on splitting the network graph into two acyclic graphs that contain all physical channels in the system. [Lysaght.P , et al] have discussed a Dynamic reconfiguration of FPGAs Dynamically reconfigurable 2-Dimensional mesh NoCs are suitable for field programmable gate array (FPGA)-based systems The partial dynamic reconfiguration of FPGAs with changing position and the number of implemented PEs and IPs, higher adaptiveness is permitted in MPSoCs during runtime [Jie Wu, et al] have explained a fault-tolerant and deadlock-free routing protocol in 2d meshes based on odd-even turn model adaptive wormhole routing algorithms for meshes without virtual channels. The model restricts the locations where some turns can be taken so that deadlock is avoided. In these we use odd – even turn model. Partially adaptive routing algorithms that are free from deadlocks. [Christophe bobda, et al] have proposed a dynamic infrastructure for communication in dynamically reconfigurable devices developed a dynamic communication infrastructure as well as

routing methodologies capable to handle routing in a noc with obstacles are created by dynamically placed components. [Thilo Pionteck, et al] have described Applying partial reconfiguration to networks-on-chip. A survey of communication architectures which allow for dynamically exchangeable hardware modules. Four different architectures are compared in terms of reconfiguration capabilities, performance, flexibility and hardware requirements.

3. EXISTING IN FIELD TEST FOR PERMANENT FAULTS IN FIFO BUFFERS BASED NOC ROUTER

In Existing method of an on-line transparent test technique for detection of faults which develop in first input first output buffers of routers during field operation of NOC. The technique is used to prevent accumulation of faults. A prototype implementation test algorithm has been incorporated into the router-channel interface and on-line test has been implemented with synthetic self-similar data traffic. In addition, an on-line test technique for the routing logic ,which considers utilizing the header flits of the data traffic movement in transporting the test patterns. The transparent test is utilized to perform online and periodic test of FIFO memory present within the routers of the NoC. Periodic testing of buffers prevents accumulation of faults and also allows test of each location of the buffer. Faulty bit will be detected inside the FIFO buffer by using single order address algorithm test (SOA).

Two level approaches in SOA test .First, it attempts to work around errors within a router by leveraging reconfigurable architectural components. Second, when faults within a router disable a link's connectivity, or even an entire router, it reroutes around the faulty node or link with a novel, distributed routing algorithm formeshes. Tolerating permanent faults in both the router components and the reliability hardware itself, it enables graceful performance degradation of networks-on-chip. Simulation results show that periodic testing of FIFO buffers do not have much effect on the overall throughput of the NoC except when buffers are tested too frequently. The existing online test technique for the routing logic that is performed simultaneously with the test of buffers and involves utilization of the unused fields of the header flits of the incoming data packets for test pattern encoding. In this paper , the existing online-test technique that can detect the run time faults , which are irregular in nature but gradually become permanent over time. The block diagram of NOC Router is shown in fig.1.

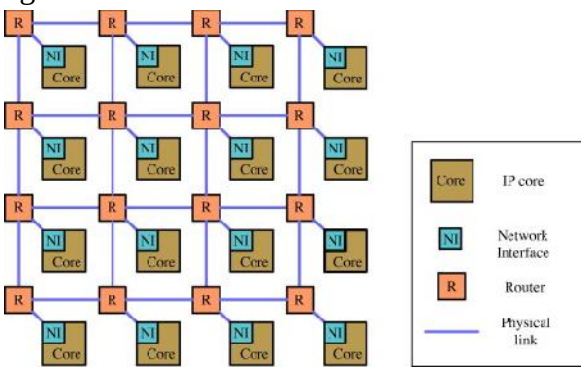

Figure.1 Block Diagram of NoC Router

The transparent SOA-MATS algorithm is intended for test of stuck-at fault, transition fault, and read disturb fault tests developed during field operation of FIFO memories. The fault coverage of the algorithm is shown in Fig. 2. In both the

figures, the word size of FIFO memory is assumed to be of 4 bits. The text in italics against the arrows indicates the operation performed, while the text in bold font corresponds to the variables used in Algorithm 1.

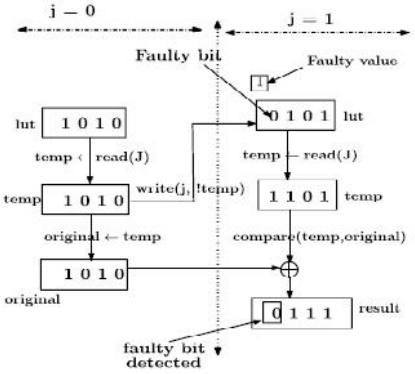

Figure. 2 SOA Test Algorithm

As shown in Fig. 2, assume the data word present in LUT be 1010.The test cycles begin with the invert phase (memory address pointer with 0 value) during which the content of location addressed is read into temp and then backed up in the original. The data written back to LUT is the complement of content of temp. Thus, at the end of the cycle, the data present in temp and original is 1010, while LUT contains 0101.Assume a stuck-at-1 fault at the most significant bit (MSB) position of the word stored in LUT. Thus, instead of storing 0101, it actually stores 1101 and as a result, the stuck-at-fault at the MSB gets excited. During the second iteration of j,when LUT is readdressed, the data read into temp is 1101. At this point, the data present in temp and original are compared (bitwise XORed). An all 1's pattern is expected as result. Any 0 within the pattern would mean a stuck-at fault at that bit position. This situation is shown in Fig.2, where the XOR of 1010 and 1101 yields a 0 at the MSB position of the result indicating a stuck-at-fault at the MSB position. However, for cases where the initial data for a bit position is different from the faulty bit value, the stuck-at-fault cannot be detected for the bit position afterthe restore phase of the test. It thus requires one more test cycle to excite such faults.

4. ROUND ROBIN ARBITER

A round-robin token passing bus arbiter guarantees fairness among masters and allows any unused time slot to be assigned to a master whose round-robin turn is later but who is ready now. A reliable prediction of the worst-case wait time is another advantage of the round-robin protocol. The worst-case wait time is proportional to number of requestors subtracted by one. The protocol of a round-robin token passing bus or switch arbiter works as follows. In each and every cycle, one of the masters has the first priority for access to a shared resource. If the token-holding master does not require the resource in this cycle, the master with the next highest priority who sends a request can be accepted the resource, and in round-robin order the highest priority master then passes the token to the next master. The structure of Round Robin Arbiter is shown in fig.3.

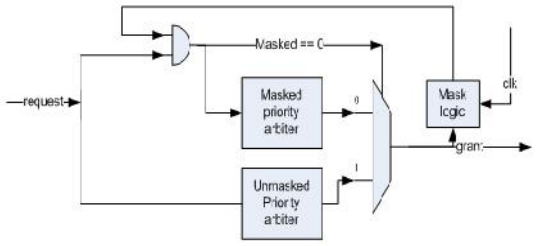

Figure 3. Structure of Round Robin Arbiter

5. PACKET SWITCHING NETWORK

Based on network characteristics, switching techniques can be classified. Circuit switched networks reserves a physical path before sending the data packets, while packet switched networks transmit the packets without storing the

entire path. Packet switched networks can classified into Wormhole, Store and Forward , and Virtual Cut Through Switching (VCT) networks. The major drawback of switching technique is a higher latency. Thus, it is not a suited switching technique for real-time data transfers. S&F switching forwards a packet only when there is enough space available in the receiving buffer to wait the entire packet. Thus, there is no need for splitting a packet into flits. This reduces the overhead, as it does not require circuits. Packet switching networks are digital networks in which large blocks of data designed by end-user processes can be damaged into smaller blocks of data called packets and sent from one network to another via routers. This networks are called packet-switched networks. In the early 1960s , the concept of packet switching was developed, and ARPANET was the world's first packet switching network. Packet switching technologies such as X.25 and Frame Relay are now used in WANs. In this type of network, there is no connection between two complete end systems, and the availability of different paths through the network rejects dependence on any single network link. Each packet has a header that contains the source and destination addresses, a sequence number that categorize the position of the packet in the real message, the length of the packets in bytes, and the total number of packets in the message. The routers on a packet switching network continuously exchange information about network topology, and the current state of the various network links. The packet switching network is shown in fig.4.

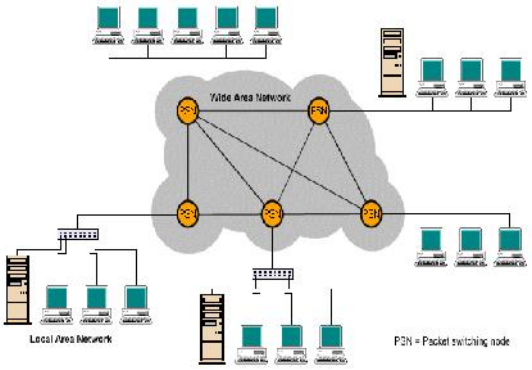

Figure.4 Packet Switching Network

6. PROPOSED NOC ROUTER BASED PACKET SWITCHING NETWORK WITH ROUND ROBIN ARBITER

In this paper, the proposed NOC router based packet switching network with round robin arbiter is designed. Packets are routed through the shortest paths and maintaining the performance of Noc in the presence of faults. This NoC router based packet switching network with round robin arbiter which is used to collect all the direction of information signal in a single direction and transfer that information from one source to another destination. Packet switching desires the use of a switching mode, which specify how packets move through the switches. Round robin arbiter is reduce the time spent on arbiter design. The arbiter plot the source and destination address from the output of buffer and develop the control signal so that input data from source side posting to the output port Arbiters are a general component in systems consisting shared resources, and centralised arbiter is a tightly integrated design for its input requests. When compared to existing method, the proposed NOC router based packet switching network with round robin arbiter gives better performance. In packet

switching the data the data carries in the form of packets between combining routers and independent routing decision is taken. The save and forward flow mechanism is best because it does not store channels and thus does not prime to idle physical channels The arbiter is of rotating priority scheme so that respective channel once get chance to transfer its data. In this router each input and output buffering is used so that congestion can be avoided at each sides. The FIFO has some different operation, they are Write Operation ,Read operation, Read and Write Operation.

The FIFO write operation is completed by when the data from input data_in is sampled at rising edge of the clock when input write enable is high and FIFO is not full. in this condition only FIFO Write operation is done.

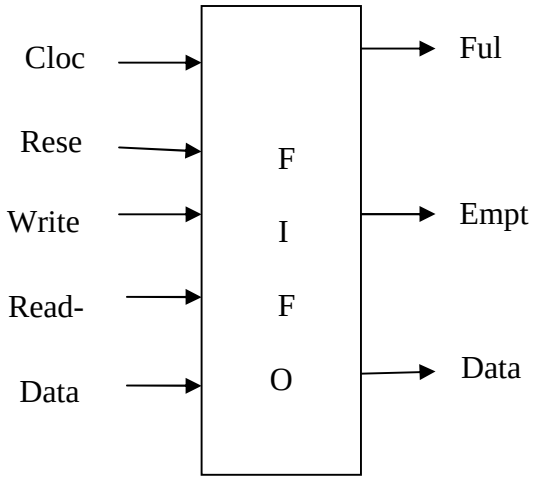

Figure.5 Functional operation of FIFO

The FIFO Read Operation is the data is read from output data out at rising edge of the clock, when read_enable is high. Full indicates that all the locations inside FIFO has been written. Empty indicates that all the locations of FIFO are empty. The fig.5 shows the functional operation of FIFO. The schematic design of proposed Network on chip (NOC) router based packet switching network with round robin arbiter is shown in fig.6.

Figure.6 schematic design of proposed Network on chip (NOC) router based packet switching network with round robin arbiter

7. RESULTS AND DISCUSSION

The design of proposed Network on chip (NOC) router based packet switching network with round robin arbiter has been designed by using Verilog Hardware Description Language (Verilog HDL).The simulation of Network on chip (NoC) router based packet switching is designed through Modelsim 6.3C. NoC takes the path from source to destination. These define the congestion less path from source to destination and the data packet routed to destination. The simulation result of proposed NoC router based packet switching network with round robin arbiter is shown in fig.7. The synthesis result (area) of proposed NoC router based packet switching network with round robin arbiter is shown in fig.8. The synthesis result (power) of proposed NoC router based packet switching network with round robin arbiter is shown in fig.9. In the proposed NoC based packet switching network with round robin arbiter, the number of LUTs are 1,046 and the number of slices are 1,191. The proposed NoC based packet switching network with round robin arbiter of power value is 0.047

watts. When compared to existing online testing technique of FIFO buffers based NoC router, the proposed NOC router based packet switching network with round robin arbiter gives better performance than existing one.

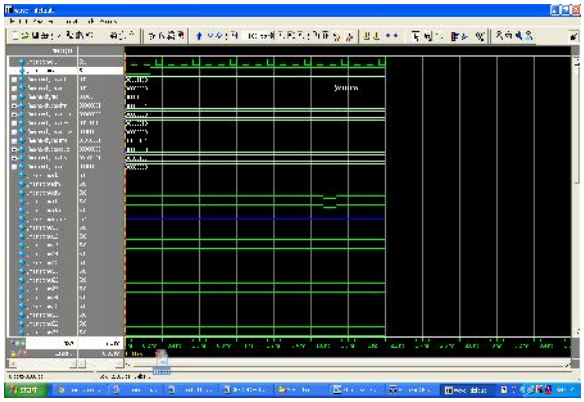

Figure.7 Simulation result of proposed NoC router based packet switching network with round robin arbiter

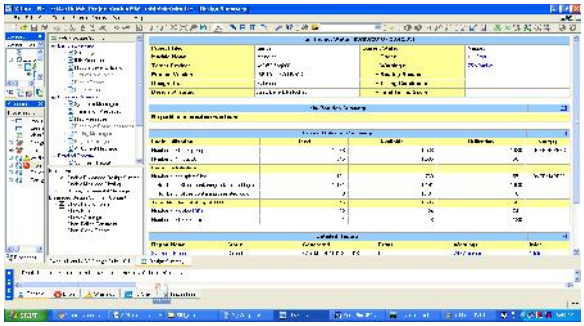

Figure.8 synthesis result (area) of proposed NoC router based packet switching network with round robin arbiter

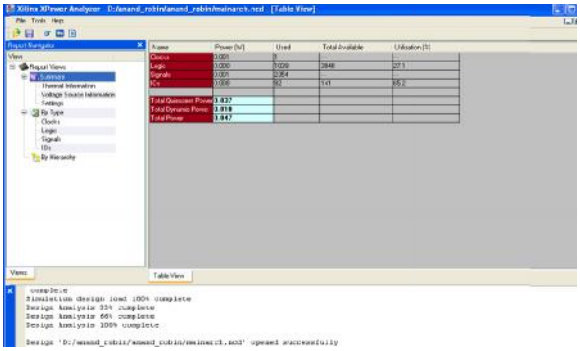

Figure.9 synthesis result (power) of proposed NoC router based packet switching network with round robin arbiter

CONCLUSION

In this paper, the proposed Network on chip (NOC) router based packet switching network with round robin arbiter has been designed through Very Large Scale Integration (VLSI) design environment. The design of advanced routing algorithm is implemented where the data packets are sent in high speed and priority based approach. The advanced router designed through Modelsim 6.3c and, the total area and power utilization is reduced through Xilinx ISE.The main aim of this design is to reduce the frequent checking of unconnected nodes and making the return path delay. Decoupling the layers of the protocol stack has the benefits over a traditional approach, such as advanced high performance bus (AHB) or Core Connect, Independent implementation and optimization of layers, Simplified customization per application, Supports multiple topologies and options for different parts of the network, Simplified feature development, interface interoperability, and scalability. In a future work, we would like to modify the proposed FIFO testing technique that will allow incoming data packets to the router under test without interrupting the test

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