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DESIGN OF EXTENDED 4-BIT FULL ADDER CIRCUIT USING HYBRID-CMOS LOGIC

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Abstract:-

This paper presents a performance analysis of hybrid 1-bit full-adder circuit design. The adder cell is dissected into smaller modules. The modules are analyzed and calculated extensively. To explore good-drivability, noise-robustness, and low-energy operations for deep sub micrometer to explore hybrid-CMOS style design. Hybrid-CMOS design style uses various CMOS logic style circuits to construct new full adders with desired performance .In this paper, a hybrid 1-bit full adder design employing both complementary metal oxide semiconductor (CMOS) logic and transmission gate logic is reported. In the proposed design of this paper first implemented for 1-bit full adder and then extended for 4 bit full adder circuit. The extended 4-bit full adder circuit has been implemented by using Tanner EDA (Electronic design automation) tool and so on. The proposed extended 4 bit full adder design is to enhance the speed of the Operation and also reduces the area, and power consumption. The new extended 4-bit full-adder circuit successfully operates at low voltages. Performance parameters such as power consumption, and layout area were compared with the existing 1-bit full adder Designs such as complementary pass-transistor logic, transmission gate adder and function-adder, hybrid pass-logic with static CMOS output drive full adder, and so on.

KEYWORDS: - Complementary Metal-Oxide-Semiconductor (CMOS), Electronic Design Automation (EDA), Arithmetic and Logic Unit (ALU).

1. INTRODUCTION

Adder is the most important critical building block in microprocessors and digital signal processors. In general, a 1-bit full adder core has three inputs and two outputs [1]. The increasing demand for low-power very large scale integration (VLSI) design can be focused at different design levels, such as the architectural, circuit, layout, and the process technology level [5]. At the circuits design level, considerable potential for power savings exists by means of correct choice of a logic style for implementing combinational circuits. The circuit logic style used in logic gates like speed, size, power consumption and the wiring net of a circuit. These designs have been broadly classified into two styles, static style and dynamic style. Static full adders are more reliable, simpler with low power requirement but the on chip area

requirement is usually larger compared to dynamic full adder. The advantages of standard CMOS style based adders are strongness against voltage scaling and transistor sizing, while the disadvantages are high input capacitance and buffers [3]. Complementary pass transistor logic is not suitable for low-power applications. Several logic styles individually have been used to design simple and complex arithmetic circuits as flip-flops, XOR-XNOR cells, full adder cells, multipliers, dividers, etc. Classical circuits design normally use only one logic style for the whole circuit design. The dynamic CMOS logic style gives a high speed of operation because the logic is built with only high mobility nMOS transistors. Due to the absence of the pMOS transistors, the input capacitance is also very low, and thus improves the speed of operation. However, it has several problems such as charge sharing and high clock load. The CMOS logic style has high switching-activity and lower noise-immunity. It consumes the power in driving the clock lines. Dynamic logic style is more susceptible to leakage [2]. In this paper, proposed a new hybrid CMOS 4-bit full adder with driving capability .The full adder consists of pass transistor logic (PTL) and static CMOS logic is called as 'hybrid full adder'. A new three-input exclusive OR is first achieved, based on PTL operation. The CMOS 90-nm process technology, the proposed 4-bit full adder is to have the minimum power consumption and less power, delay product by SPICE simulation.

2. LITERATURE SURVEY

[A.M. Shams, et al, 2002] presented the performance analysis of low power 1-bit CMOS full adder cells. The adder cell has been divided into three constituting modules. Different designs for each of these modules have been implemented, simulated, analyzed, and compared in these papers. Twenty different 1-bit full-adder cells are constructed and designed by connecting the combinations of different modules. Each of these cells shows different power consumption, speed, area, latency and driving capability figures. Two realistic circuit structures that include full adder cells are used for simulation. Full-adder cells are developed and presented to the circuit designers to pick the full-adder cell that satisfies their specific applications. [D. Radhakrishnan, 2001] explained the low-voltage low power CMOS full adder. XOR and adder cells that have appeared in the latest literature use pass transistors and transmission gates are designed by ad hoc techniques. The formal design methods for these circuits using k-maps and pass network theorems are presented. A new six-transistor XOR-XNOR cell is designed , by using this formal approach that does not affect from the threshold voltage drop in MOS transistors, but at the same time fewer transistors are used compared to existing designs. However, more design effort is required for the sizing of the transistors. The new cell can easily be accepted for low- voltage operation as well as the supply voltage is not allowed to fall below $2\times|Vtp|$. A full adder design using the new XOR-XNOR cell .Further work is in proceed to program the design of the XOR-XNOR cell so that the transistor sizing can be spontaneously evaluated based on the speed-power requirements. [S. Goel, et al, 2006] explained the design of robust, energy-efficient 1 bit full adders for deep submicrometer design using hybrid-CMOS logic style. Hybrid-CMOS design style provides more freedom to the designer to choose different modules in a circuit depending upon the application. Using the adder categories and hybrid-CMOS design style, many full adders can be developed. For an example, a novel 1-bit full adder designed using hybrid-CMOS design style is presented in this paper. The proposed hybrid-CMOS full adder has better performance than most of the standard full-adder cells. It performs well with supply voltage scaling and under different load conditions. When embedded in a four-operand CSA, it outperforms all the other adders making it suitable for larger adder. [C.K.Tung, et al, 2007]

described a low-power high-speed CMOS full adder core for embedded system. Based on a new three-input 3-XOR design, the new hybrid full adder is consists of pass-transistor logic and static CMOS logic. The important design objectives for the full adder core are providing not only low power consumption and high speed but also with driving capability. The transistor count of Transmission Full Adder is 26, while the conventional CMOS full adder needs 28 transistors. Transmission Full Adder gives buffered outputs of the proper polarity for both sum (S) and carry-out (Co). And the disadvantage of the design is slow speed and high power consumption. [M.Zhang, et al, 2003] explained novel hybrid-pass logic with static CMOS output drive full adder cell. The pass logic style has been used to efficiently generate the XOR and XNOR functions instantaneously and a good drivability carry out have been generated by a novel complementary CMOS style with regular structure. The circuit has shown to be power-delay efficient over a wide supply voltage ranges above 2.4V and is therefore suitable for constructing low power, high performance arithmetic logic unit for embedded applications.

3. HYBRID ADDER CELLS

The hybrid adders were designed using conventional implementing methods, they use only transistors and not use input capacitors. The Chang adder [6] has 26 transistors and it utilizes a modified low-power XOR or XNOR circuit. In this circuit worst case delay problems due logic transitions are solved by adding more transistors, however, these extra transistors increase the power consumption of the full adder cell. The Aguirre adder [11] utilizes the Swing restored complementary pass-transistor style and in alternative logic structure in order to obtain balanced paths which is based on the multiplexing of the Boolean functions XOR or XNOR and AND or R, to find the SUM and CARRY outputs respectively. The Goel adder [12] use a XOR–XNOR circuit that generates balanced full-swing outputs. It has high-speed operation due to the cross-coupled pMOS pull-up transistors providing the intermediate signals fastly and a hybrid-MOS output stage with a static inverter at the output. The Agarwal adders[13] use the CPL logic. This adder is mainly composed by NMOS transistors with pull–up PMOS transistors to find the full swing output voltage. Due to positive feedback and use of NMOS transistors, the circuit is inherently fast. This hybrid adder has a balanced structure with respect to generation of 'SUM' and 'CARRY OUT' signals. This helps in instantaneous arrival of signals in tree structured circuits.

4. THE FULL-ADDER CATEGORIZATION

Hybrid CMOS full-adder cells are broadly three categories depending upon their structure and logical equation of the sum output. The sum and carry (C_{out}) outputs of a single - bit full adder generated from the binary inputs A, B, and C_{in} can be generally equated as

$$SUM = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = A.B + C_{in}.(A \oplus B) \quad (2)$$

These outputs can be explained in many different logic expressions and thereby, calculate the structure of the circuit. The different possible structures for full adders are classified into three broad categories.

XOR-XOR based Full Adder:

The Sum and Carry outputs are generated by the following equation, where H is A⊕B and H' is the complement of H.

$$SUM = A \oplus B \oplus C_{in} = H \oplus C_{in} \quad (3)$$

$$C_{out} = A.H' + C_{in}.H \quad (4)$$

XNOR-XNOR –Based Full Adder:

The Sum and Carry outputs are generated by the following expression

$$SUM = \overline{\overline{(A \oplus B)} \oplus Cin} = \overline{H' \oplus Cin} \quad (5)$$

$$C_{out} = A.H' + C_{in}.H \quad (6)$$

Centralized Full Adder:

The sum and carry outputs are generated by the following expression.

$SUM = H \oplus C_{in} = H.\ C'_{in} + H'.\ C_{in}$ (7)

$C_{out} = A.\ H' + C_{in}.\ H$ (8)

5. DESIGN APPROACH OF EXISTING 1-BIT FULL ADDER CIRCUIT

The Existing single-bit full adder circuit is designed by using Complementary Pass transistor logic, Transmission gate logic and hybrid pass-logic with static CMOS output.These are the most important logic styles in the conventional domain. These logic circuits are implemented by tanner EDA tool. These different logic styles which is used to improve the overall performance of the full adder. The complementary pass transistor logic shows a good voltage swing restoration employing 32 transistors. However, complementary pass transistor is not a correct choice for low-power applications. Because of its increased switching power, Number of transistor count is high. The disadvantages of complementary pass transistor logic is the voltage degradation was successfully addressed in TGA, which uses 20 transistors for full adder implementation and also drawbacks of CPL like slow speed and high power consumption. In a Hybrid pass logic with static CMOS circuit, XOR and XNOR functions were instantaneously generated by pass transistor logic module by using only six transistors and employed in CMOS module to produce full swing outputs of the full adder but at the cost of increased transistor count and decreased speed. The hybrid logic styles offers promising performance, and the logic adders suffered from bad driving capability issue and their performance degrades in the cascaded mode of operation if the suitably designed buffers are not involved. The existing Single-bit full adder which is used to reduce the area, power and latency of the circuit.

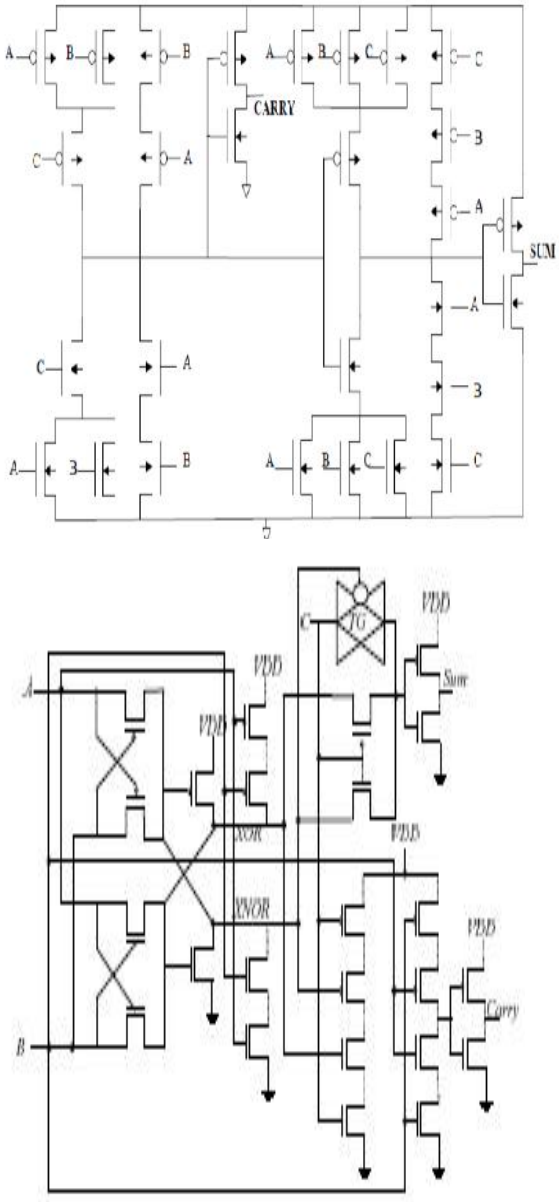

Figure.2 Structure of Hybrid full adder

6. PROPOSED EXTENDED 4-BIT FULL ADDER CIRCUIT

The proposed extended 4-bit full adder circuit with CMOS technology is designed by using Tanner EDA tool. In this paper, 1-bit full adder is extended to 4-bit full adder. The proposed extended 4-bit full adder circuit, reduces the area, delay and power were compared with existing designs such as complementary pass-transistor logic, transmission gate adder, hybrid pass-logic with static CMOS output drive full adder. In the proposed structure, the numbers of transistor counts are decreased and also improve the overall performance of the circuit. In the proposed

4-bit full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit.

This XNOR module is designed to minimize the power to the possible extend with avoiding the voltage degradation possibility. The single bit full adder cell designed for optimum performance may not perform well under deployment to real-time conditions. So the single bit adder cell is extended to 4-bit full adder cell to perform well in real time applications.

The circuit diagram of extended 4-bit full adder circuit I s shown in fig.3.

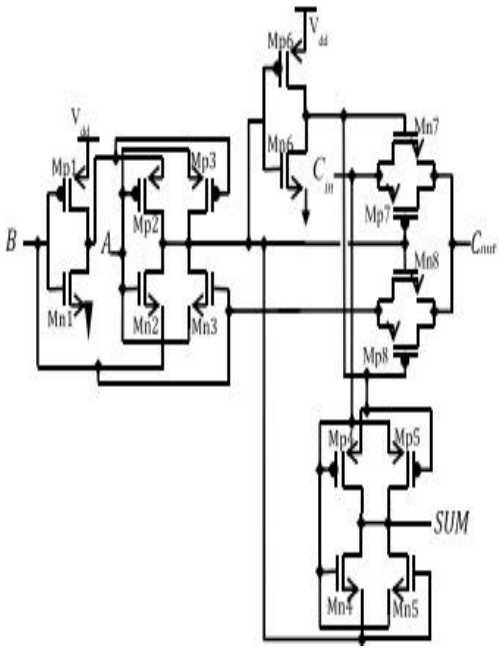

Figure.3 Circuit diagram of proposed full adder circuit

7. RESULTS AND DISCUSSION

The proposed designs of extended 4-bit full adder circuit with CMOS technology have been implemented by using Back End Tanner Electronic Design Automation (EDA) v14.1i tool. The schematic design of extended Full adder circuit is shown in fig.4.

The Waveform of proposed extended 4-bit full adder circuit is shown in fig.5. By using tanner, it will reduce the area and power consumption and also improves the performances of the full adder cells.

The number of MOSFETS are 104, the number of voltage sources are 10, model definitions are 2, independent nodes are 56, total number of nodes are 67, MOSFET geometrics are 2, computed models are 2 and the boundary nodes are 11. The power value of extended 4-bit full adder circuit is 0.0639 watts.

The output waveform of power for extended 4-bit full adder circuit is shown in fig.6. In table 1, shows the comparison of full adder logics.

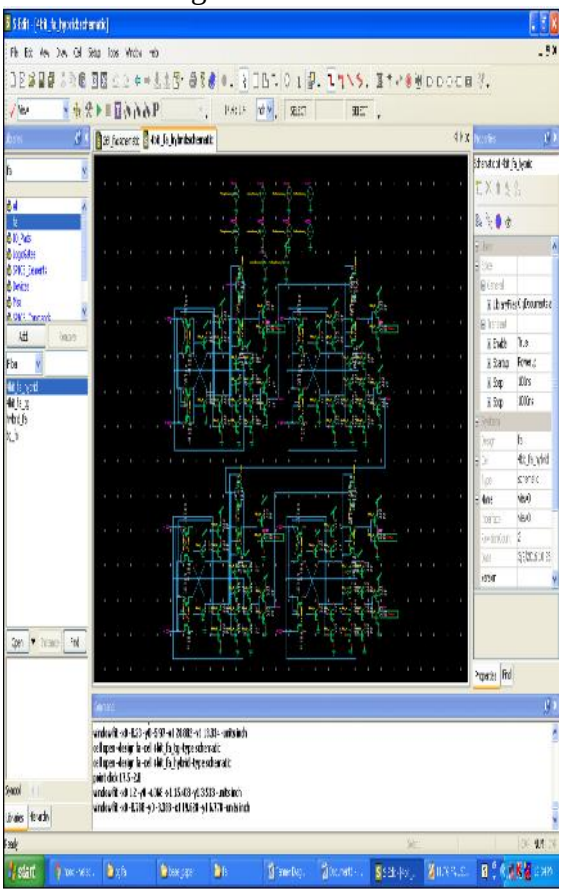

Figure.4 Schematic design of extended 4-bit full adder circuit

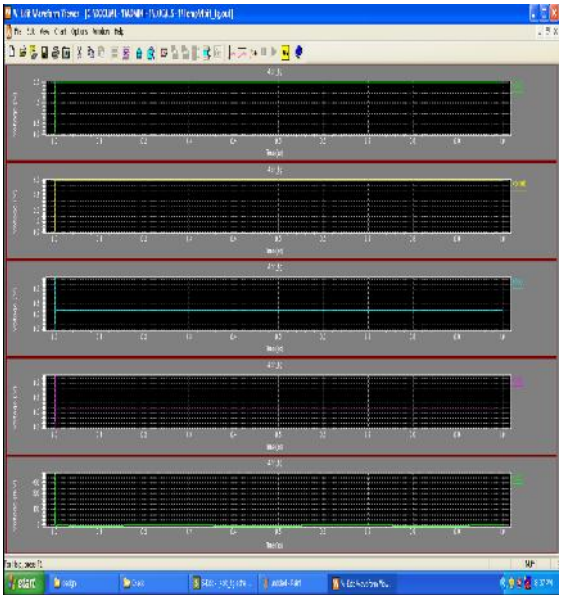

Figure.5 Waveform of proposed extended 4-bit full adder

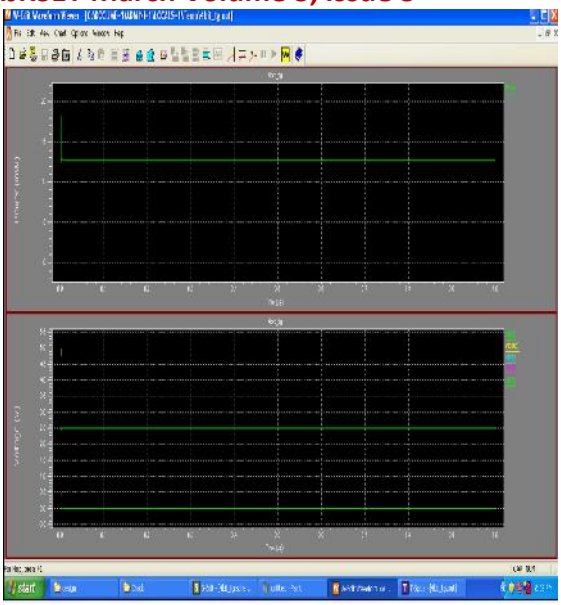

Figure.6 Output waveform of power for extended 4-bit full adder

Cell Name	Number of Transistors	Area Analysis	Power Analysis
Complementary Pass Transistor Logic	32	32	8.939
Transmission Gate Full Adder	20	20	8.179
Conventional CMOS Logic	28	28	9.209
Hybrid Full Adder Logic	20	20	2.190
4-bit Full Adder	104	10	0.0639

Table 1.Comparison of Complementary

Pass Transistor Logic, Transmission Gate Full Adder,Conventional CMOS Logic, Hybrid Full Adder and 4-bit Full Adder Logic

CONCLUSION

In this paper, Extended 4-bit full adder circuit is designed using tanner EDA tool through Very Large Scale Integration (VLSI) System design Environment. Less area utilization , and lower power consumption are the important key factors in VLSI System design environment. The circuit was designed by using tanner EDA tool with CMOS technology and compared with other standard designs like CMOS, CPL, TFA, TGA and other hybrid designs. The extended 4-bit full adder circuit offers less power value .The proposed full adder was further used to implement 32-bit carry propagation adder having buffers at appropriate adder stages. When compared to single-bit Ful adder , the proposed extended 4-bit full adder gives the better performances. These full adder circuit is used to improve the overall performance of the structure.

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