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An Optimized Fused Add-Multiply (FAM) Operator

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Abstract:-

Now a day's Digital Signal Processing (DSP) are widely used by many manufacturers in Integrated Circuit (IC) and Embedded Industries. The commonly used functional units in the DSP Processors are controller unit, memory unit, Arithmetic logical unit (ALU). ALU unit will consist of MAC unit, MAD unit. Large number of arithmetic operations are carried out by DSP processors of which mostly used operator is Add-Multiply (AM). Here we mainly focus on fusion of add unit and Modified Booth (MB) unit, thereafter called as Fused Add Multiply (FAM) unit which is used for recoding in multiply operation. A Wallace Carry Save Adder (CSA) tree is used to reduce delay for addition of partial products. The overall result is generated by a Carry Propagate Adder (CPA). Comparing with the existing system, the proposed system yields considerable performance in critical delay, power consumption, and area.

Index Terms: - Fused Add-Multiply operation, Sum to Modified Booth (SMB) Recoding, Partial Product Generator, Wallace Carry Save Adder (CSA) Tree, Carry Propagate Adder (CPA).

1. INTRODUCTION

With the advancement of signal processing systems like communication and multimedia systems, the real-time signal processing like audio processing and image/video processing large, fast and accurate data processing units are being demanded day-by-day. As most of the Digital Signal Processing (DSP) Processors use Add-Multiply (AM) unit in processing intensive kernels such as Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), Finite Impulse Response (FIR) filters and signal convolution.

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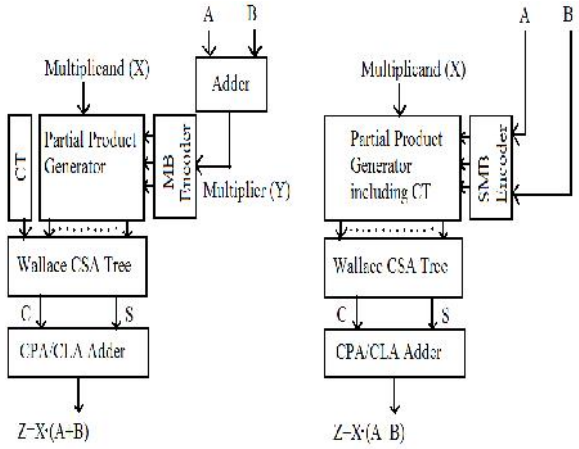
Bujjibabu Penumutchi is with Aditya Engineering College as Assistant Professor in ECE Department whose primary of interest is low power VLSI Design (e-mail:bujjibabu82foru@gmail.com) The straight forward design of Add-Multiply (AM) unit (Fig.1) is by giving two inputs to be added to the adder, driving its output to Modified booth (MB) Encoder, driving its output to partial Product Generator (PPG) where multiplicand is modified according to the signals from MB encoder, driving its output to a CSA tree to add all the partial products, finally a Carry Propagate Adder (CPA)/Carry Look Ahead (CLA) adder is used to generate final product. In this fused system (Fig. 1) we require pre-processing step of re-coder in order to represent the operands in carry save form. In [1] the author proposes a re-coder for this purpose, we call it as Sum-to-Modified Booth (SMB) re-coder. The two inputs A & B are given as inputs to the SMB re-coder, The three signals from SMB re-coder are for sign, 1*multiplicand and 2*multiplicand is used for PPG to generate Partial Products with correction term in it. Correction term is generated for adding both positive and negative (2's complement) type of numbers. As CSA is

most commonly used for addition by implementing the Wallace tree technique the complexity for addition is decreased, because of Wallace tree structure the operation is processed in parallel. Here by use of counters like 3:2 counter, 4:2 counter etc., the parallelism occur sand critical delay can be reduced. By giving the outputs from Wallace tree to CPA/CLA circuits we will get the final result. The most effective way to increase the speed of the multiplier is to reduce number of partial products because the multiplication precedes a series of additions. By using Modified Booth Algorithm (MBA) the number of partial products to add can be reduced. There is a relation for how many bits to be inspected (n) with reference to radix (r).

$$n = \log_2 e \qquad (1)$$

For example if this work is doing for radix-4 the number of bits to be inspected is 3. By inspecting 3-bits at a time with one bit as reference bit fir each cycle 2 bits get eliminated for next cycle.



(a) (b)

Figure 1: Add-Multiply operator based on (a) Conventional design and (b) Proposed design.

2. MOTIVATION

The conventional design of AM operator will have two inputs A & B given to an adder and result will be Multiplier (mp). Multiplier (mp) = (A + B) = Y. The multiplier is recoded into its MB form. These signal along with Multiplicand (mc) = X is driven to the PPG where we get the product terms = X · Y. The drawback is by using separate adder will insert significant delay in critical path of circuit. An optimised design of AM operator is based on fusion of adder and MB encoding unit. By directly recoding the two input's A & B equivalent to MB representation of multiplier will reduce significant delay. For our convenience we can use CLA in the SMB unit. By fusing this Correction term in the PPG the area related to this circuit is also get reduced.

3. IMPLEMENTATION

A. SMB Encoder

In SMB encoder we recode four consecutive input bits (two from A & two from B) into one MB digit which is represented using (sj, xj, 2xj) for radix-4 operation. In [2] the author proposes a full adder circuit (Fig. 2) which is modified for his convention. With that he has made a SMB unit using recoding cell (Fig. 3).

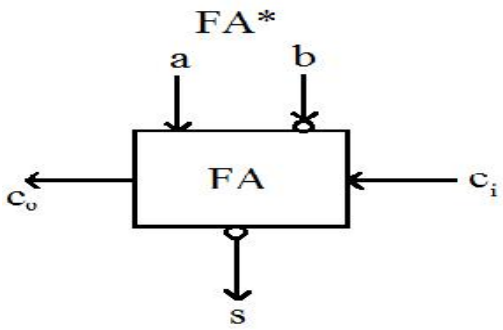


Figure 2: A modified Full adder circuit called as fa*

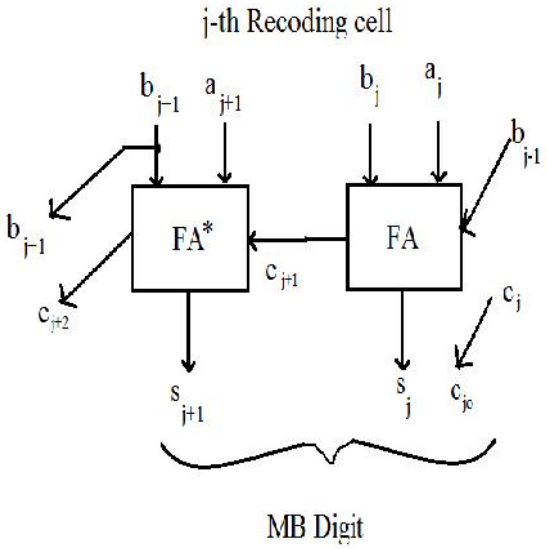


Figure 3: SMB recoding unit using j-th Recoding cell

B. Partial Product Generator including correction term

The Partial Product Generator (PPG) is used to generate partial products using the MB form. The MB form includes three signals they are sign, 1j and 2j. With these signals we get the recoded digit by formula stated below.

$$Y_j^{MB} = (-1)^{sj} \cdot [1_j + 2_j] \quad (2)$$

In technical terms to represent the partial product of multiplicand (A) the operation to be performed on the multiplicand will be shown below (Table 1) and the logic circuit to implement PPG is also given below (Fig. 4).

MB Recoded Digit	Operation on multiplicand Abefore shifting 2-bits to right
0	Nothing
+1	Add A to existing sum of partial products (SPP)
+2	With a left shift on A add to existing SPP
-2	2's compliment With a left shift on A add to existing SPP
-1	2's compliment add A to existing SPP

TABLE 1: Operation on multiplicand with MB digit

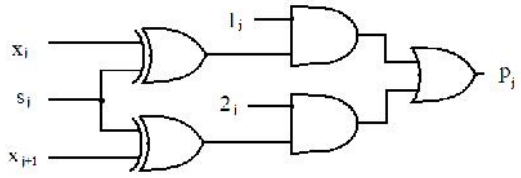


Figure 4: Partial Product Generator fir j-th cell

C. Wallace Carry Save Adder (CSA) tree

The Wallace CSA tree will have inputs from the PPG block at same time. In each column all the partial products are added together by a set of parallel counters like 3:2, 4:2, 5:2, 6:2, 7:2 etc. counters. This set of counters will reduce the new matrix until a two-row matrix is generated. The final results are added using CPA. In comparison to the basic array multiplier, the delay of summing partial products in a column is O(log(n)) rather than O(n). Wallace tree is a summation of method and it used in conjunction with fixed-width booth multiplier to increase computational speed. The Wallace tree algorithm to compute adder structures are shown in (Fig. 5-7).

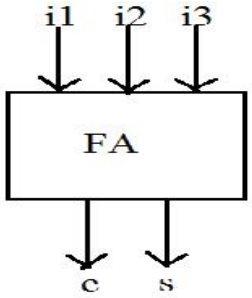


Figure 5: 3:2 Compressor

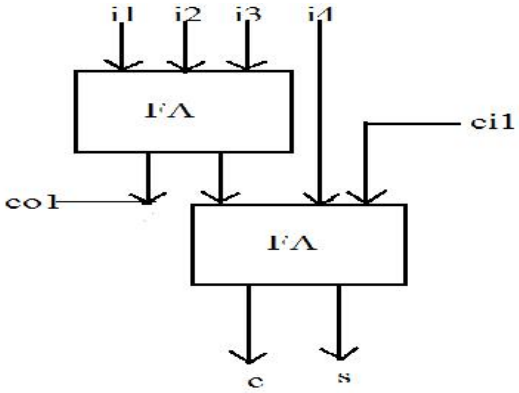


Figure 6: 4:2 Compressor

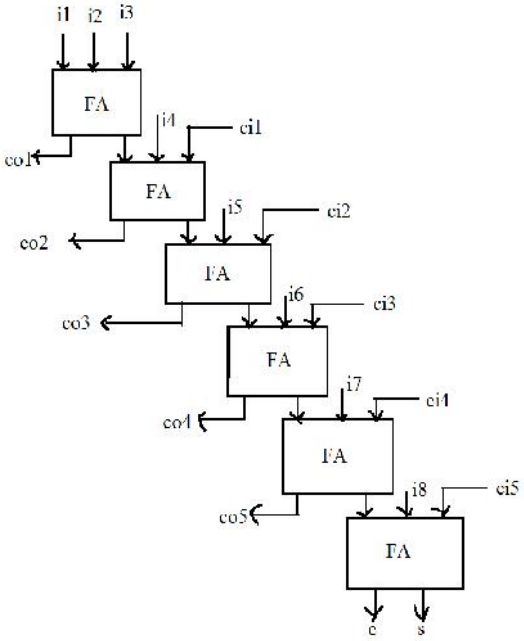


Figure 7: 8:2 Compressor

D. Carry Propagate Adder (CPA)

The Carry Propagate Adder (CPA) is used where we need to propagate the carry to the next level. The figure (Fig. 8) shows the CPA example circuit. The figure clearly shows that the carry bit ripples through the chain of cascaded full adders from lower bit to higher bit. It is the less area occupying adder of all the adders, but delay depends on carry chain from lower to higher bit order.

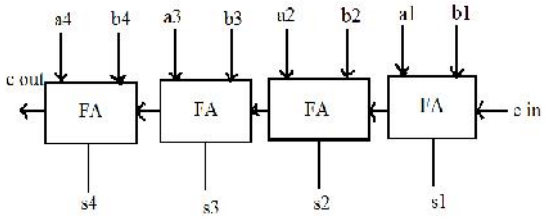


Figure 8: Carry Propagate Adder

Alternatively we can use Carry Look Ahead (CLA) adder in place of CPA where the speed of operation is more issue, but the area occupancy of CLA adder will be more because of more logic circuit. The Correction Term (CT) can be directly generated by taking the MSBand modifying this bit. By combining all these four units we have designed will give the expected results with the optimised performance.

4. SYNTHESIS, SIMULATION AND DISCUSSION.

The circuit Synthesis and Simulation were carried out using random input vectors Xilinx Synthesis Technology (XST) and ISE Simulator (ISim) in Xilinx ISE Design Suite v12.2. I have designed it for 16-bit operation so assumed the inputs would be A, B, mc (multiplicand). First the A & B inputs are given to the SMB encoder which gives the outputs in MB representation i.e. sj (sign), xj (1j) and xj2 (2j). The Institute of Electrical and Electronics Engineers (IEEE) standard symbol (Fig. 9) and simulation results (Fig. 10) are shown in figures.

Next, the outputs from the SMB Encoder are driven to the Partial Product Generator (PPG) block and the outputs would be the partial products i.e. mmc1 to mmc8 in the figure. The IEEE symbol (Fig. 11) and simulation results (Fig. 12) are shown in figures.

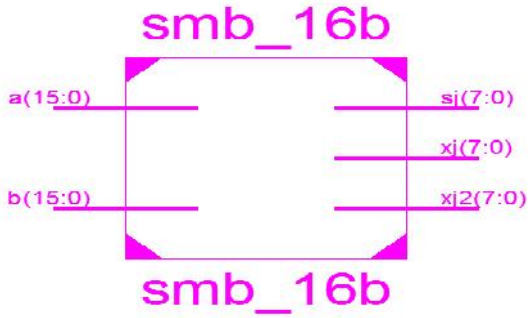


Figure 9: SMB Encoder standard symbol

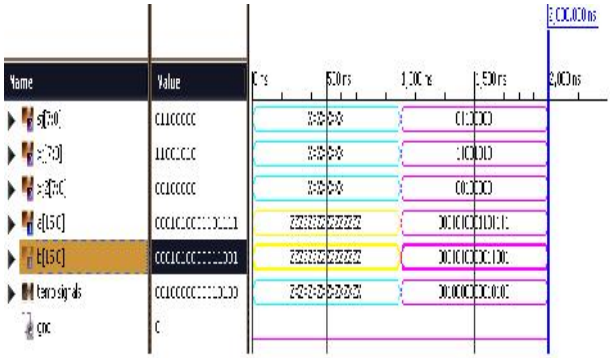


Figure 10: SMB Encoder Simulation results

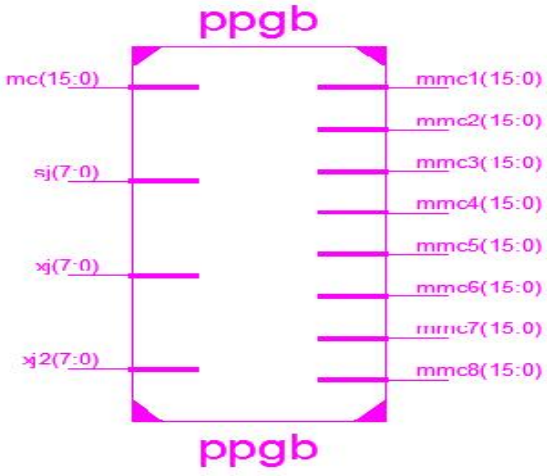


Figure 11: Partial Product Generator Standard diagram

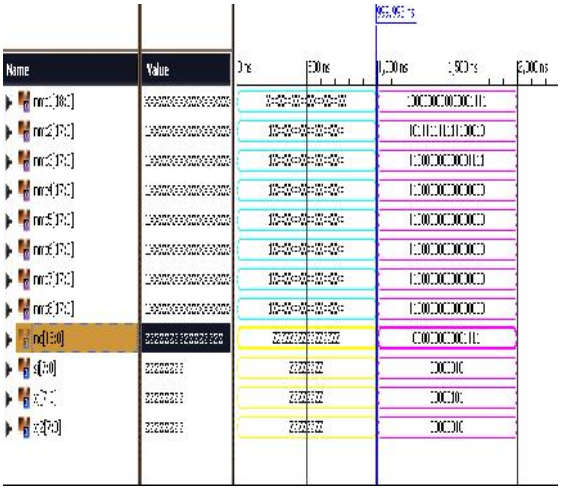


Figure 12: Partial Product Generator Simulation results

The simulation results up to know from the proposed circuit are exactly what we are expecting. As expected the synthesis report also showing the increased performance. As I have designed a Wallace CSA tree its results are not expected so there is some errors in the circuit to be modified.

5. DESCRIPTION

This proposed circuit is meeting the requirements to implement these structure in Spartran-3E starter board kit. It can also be verified by on board using Xilinx Chipscope Pro. The power analysis is done in XPower Analyser. The critical delay can be known by using Xilinx Timing Analyser.

6. EVALUATION

We have simulated the design and we got the results as shown in Table 2. The results will show up to the PPG block only because we have done up to there correctly. The next blocks are designed but there are some errors in it the results are not as expected. So we are trying to modify the circuit performance.

Design	Performance Results		
	Area (%)	Delay (ns)	Power (mW)
SMB	1	8.864	81
PPG	5	10.654	81

TABLE 2: Performance Results

CONCLUSION

Add-Multiply (AM) is the basic operator in the multimedia and communication systems for implementation of functions like DCT, DWT, FIR filters etc. This paper focuses on fusion of Adder and MB encoder units, Generating Correction Term (CT) in the same PPG block. This optimization leads to the improvement in the performance characteristics like reduced critical delay, reduced area, and obviously power dissipation. By incorporating these designs in DSP processor will yield considerable performance improvement.

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