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Design and Implementation of a Novel Bi-Recoder Based Digital FIR Filter

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Abstract:-

In this paper, an efficient direct form Finite Impulse Response (FIR) filter is designed to enhance the speed and throughput of digital filtering mechanism. Multiplication and Accumulation (MAC) units are to be recognized as high potential for the design of FIR filter. To enhance the performances of MAC unit for digital FIR filter, a novel Bi-Recoder based multiplier is developed in this paper through Very Large Scale Integration (VLSI) System design environment. Less silicon area utilization, lower power consumption and high speed are the main concerns of VLSI System design. Reduced complexity Square Root Carry Select Adder (SQRT CSLA) is one of the best digital addition mechanisms to perform the accumulation of two large N-bit binary values. In this research work, reduced complexity SQRT CSLA is to be considered to support the addition process of Bi-Recoder multiplier. Finally, the design of a novel reduced complexity SQRT CSLA based Bi-Recoder multiplier is incorporated into digital FIR filter to enhance the performances of filtering mechanisms in terms of VLSI concerns. Proposed model of digital FIR filter utilizes the less hardware and high speed than other best existing model of digital FIR filters.

Keywords: - Multiplication and Accumulation (MAC) unit, Finite Impulse Response (FIR) filter, reduced complexity Square Root Carry Select Adder (SQRT CSLA), Bi-Recoder based Multiplier, Very Large Scale Integration (VLSI).

1. INTRODUCTION

Digital Signal Processing (DSP) operations are widely used in wireless communication Technologies to control and guide the signal flows. Convolution, Correlation, Frequency Transformation and filtering are the important operations of DSP applications. In this research work, Finite Impulse Response (FIR) filter is considered for improving the performance of digital filtering process in wireless communication technology. Large endeavours have been worked on direct form digital FIR filter to improve the performance in terms of high speed and throughput. The relationship of input-output of Linear Time Invariant (LTI) System is represented as in equation (1),

$$y_{out}(n) = \sum_{p=0}^{N-1} Coeff_{p}\, x_{in}(n-1) \qquad (1)$$

Where, $x_{in}(n)$ represents the input samples of FIR filter, $y_{out}(n)$ represents the output samples of FIR filter, N is the order of the filter or length of the filter and $Coeff_p$ denotes the coefficient of filters. Impulse response of FIR filter must be finite and therefore, filtrations also based on some finite numerical values. Periodical multiplication and accumulation structures are used to maintain the impulse response of FIR filter as finite. Square Root Carry Select Adder (SQRT CSLA) is one of

the best VLSI based adders, because it utilizes less hardware complexity and high speed. In [4], area efficient CSLA architecture is developed for binary addition process. The combination of Ripple Carry Adder (RCA) and Binary to Excess1 Conversion (BEC) unit is used in [4] to reduce the propagation delay of addition process. In SQRT CSLA, N-bit data can be divided into $\sqrt{N}$ groups for performing parallel addition process. In [8] and [7], group structures for N-bit BEC based SQRT CSLA are explained with necessary diagrams. Reduced complexity Wallace multiplier is developed in [5] for the design of digital FIR filter. In reduced complexity Wallace multiplier, the partial products are arranged in an inverted triangle order. The matrix of triangular order outputs are divided into three row groups. Full Adders (FAs) are used for adding three bits and Single bit and a group of two bits are moved to the next stage directly. In final stage of Wallace tree multiplier require sufficient N-bit binary adder for performing accumulation operation. In [9], Efficient CSLA circuit is used for addition part of reduced complexity Wallace multiplier. Parallel Prefix Han-Carlson Adder is used in [10], for addition part of reduced complexity Wallace multiplier. Also in [6], both reduced complexity Wallace multiplier and CSLA circuits are incorporated into digital FIR filter. Different types of multipliers are used in various literatures to design FIR filter. For instance, in [1] and [2], extended double base number system is used for designing a low complexity programmable FIR filter. Similarly, Multiple Constant Multiplication (MCM) technique is used in [3] for multiplication part of digital FIR filter.

In this work, design of FIR filter is done by using Verilog Hardware Description Language (Verilog HDL). To increase the performance of digital FIR filter, a novel Bi Recoder Multiplier and reduced complexity SQRT CSLA are developed in this research work.

2. BI-RECODER MULTIPLIER

The partial product generation is the first method of any multiplier. According to array multiplier, N^2 AND gates are used to provide partial product generation. On the other hand, 2:1 Multiplexers are used to provide partial product generation. Multiplicand value is directly given to one of the input of 2:1 Multiplexer and N-bit of zero's are given to another input of 2:1 Multiplexer. Multiplier value is given to the selection line of multiplexer value. For instance, 8-bit multiplier requires 8 multiplexer to provide the partial product results. In every stage, single bit of multiplier is considered as selection input of Multiplexer. If it is zero, Multiplexer simply passes '0' to output else if it is one, Multiplexer passes the multiplicand value to output. In this paper, Multiplexer based partial product generation technique considered as a basement tutorial for designing a novel Bi-Recoder multiplier. In every stage of Bi-Recoder multiplier, two bits of multiplier value are considered as selection input. If it is '00' means, Multiplexer simply passes'0' to output else if it is '01' means, Multiplexer passes the multiplicand value to output else if it is '10' means, Multiplexer passes the 1-bit left shifted value of multiplicand to output else it is '11' means, Multiplexer passes the addition value of multiplicand and 1-bit left shifted value of multiplicand to output. In this way, Bi-Recoder multiplier produces the partial product values effectively. For instance, 8-bit multiplier requires only 4 multiplexer to provide partial product generation. Hence, hardware complexity of Bi-Recoder multiplier reduces effectively. Fig. 1 illustrates the partial product generation of Bi-Recoder multiplier. In this example, 8-bit multiplier is considered. In fig. 1, 'a' represented as 8-bit Multiplicand value and 'b' represented as 8-bit Multiplier value. In each stage, 9-bit partial product output is generated under the condition of selection inputs. Further, Wallace tree reduction method is used to reduce the 4-rows of partial product generation values into 2-rows of partial product generation values. Hence, the partial product generation circuit of Bi-Recoder absolutely reduce the hardware complexity, delay and power consumption of multiplier.

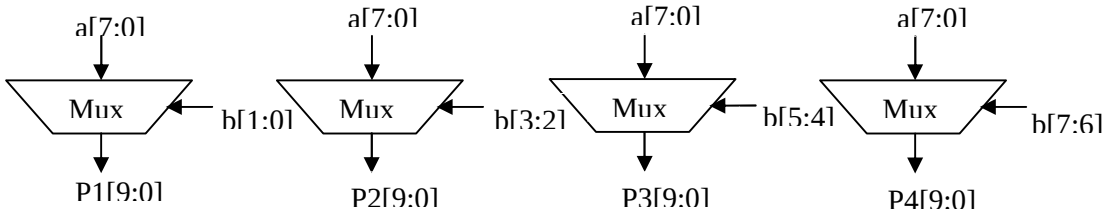

Figure 1: Partial product generation of Bi-Recoder Multiplier

However we cannot decide the best performance with help of only partial product generator circuit, because the performance of any multiplier depends on both partial product generation and types of adder used for adding the partial product generation values. Therefore, an area efficient and low power adder structure also required to increase the performance of Bi-Recoder multiplier. Reduced complexity SQRT CSLA adder is designed in this paper to increase the performance of novelty of Bi-Recoder multiplier.

3. REDUCED COMPLEXITY SQRT CSLA

Ripple Carry Adder (RCA) is one of the basic VLSI based adders which is largely affected by Carry Propagation Delay (CPD). To reduce the CPD of circuit, Carry Select Adder (CSLA) is developed in past. In CSLA circuit, N-bit data is divided into $\sqrt{N}$ groups to provide the parallelism. Hence, this circuit is named as SQRT CSLA. Divided each and every group can operate instantly at same time. However, RCA circuits of SQRT CSLA reduce the performance in terms of speed. Hence, one set of RCA circuits is replaced by BEC circuits (have same functionality with less number of gates) to increase the speed of the adder significantly. The circuit diagram of 16-bit BEC based SQRT CSLA circuit is illustrated in fig. 2. Every group structures have RCA, BEC and Multiplexer circuits, hence most essential components to design group structures of SQRT CSLA are Full Adders (FAs), Half Adders (HAs), Logic Gates (AND, EX-OR and NOT) and Multiplexers. For instance, group-2 and group-3 structures of 16-bit SQRT CSLA circuits are illustrated in fig. 3. In this structures, combination of FA and HA gives the results of RCA and it is followed by BEC circuit which indicated in dotted line of fig. 3. Finally, Multiplexors are used to provide final sum outputs. Carry input (C_{in}) is given to the selection input of first group of Multiplexers. Remaining groups get the Carry inputs from previous groups. Hence, final stage of SQRT CSLA only cause little CPD than traditional RCA circuit.

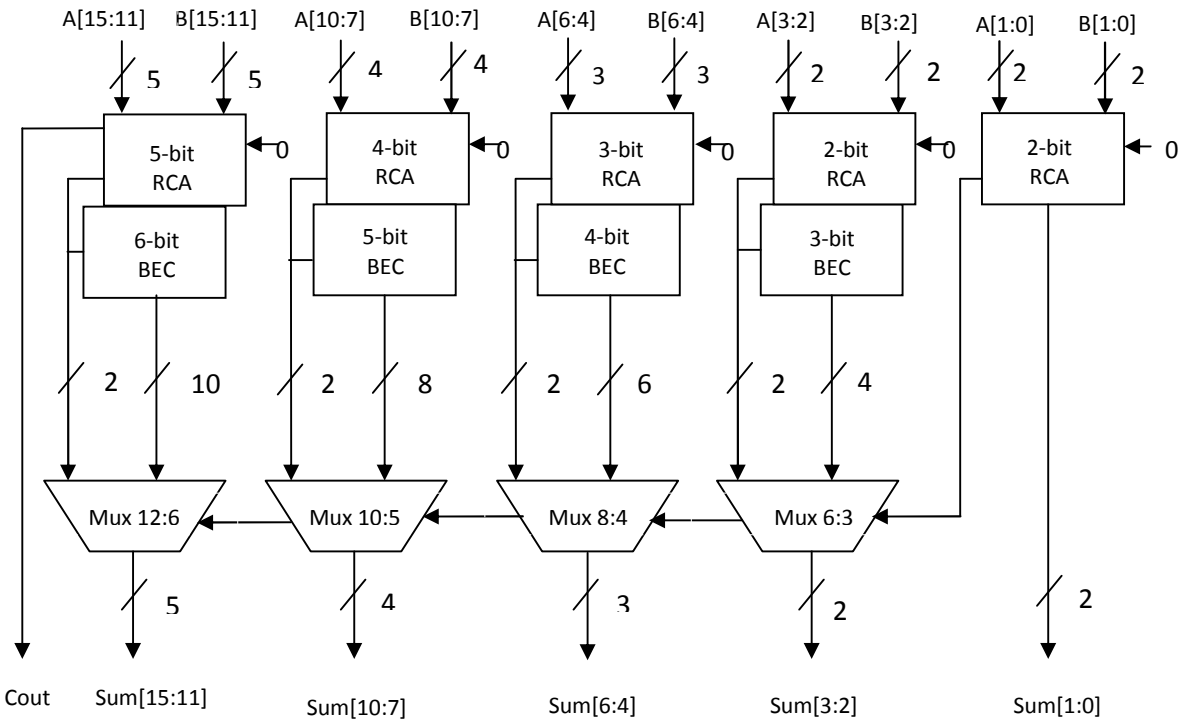

Figure 2: Architecture of 16-bit BEC based SQRT CSLA

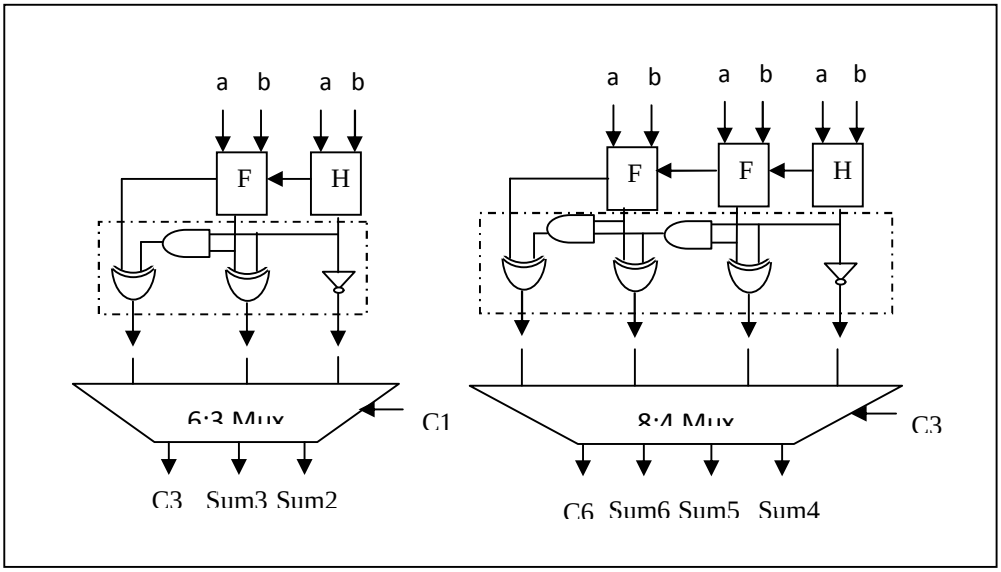

Figure 3: Group-2 and Group-3 Structure for 16-bit SQRT CSLA

In this paper, the complexity of BEC circuits and multiplexer circuits are realized and re-constructed to increase the performance in terms silicon area and power consumption. Redundant logic function of each group structures are identified and eliminated to reduce the hardware complexity. Hence, the developed adder circuit is named as "Reduced Complexity SQRT CSLA". The circuit diagram of reduced complexity SQRT CSLA for 4-bit addition (group-4 structure) is illustrated in fig. 4. Similarly, we can extend and compress the circuit of fig. 4 for group-5 structure and group-2, group-3 structures. When compared to the traditional group structures of BEC based SQRT CSLA, developed group structures of reduced complexity SQRT CSLA reduces the gate count value significantly. Gate count for traditional group structures of SQRT CSLA and developed group structures of reduced complexity SQRT CSLA are demonstrated in table 1. Theoretically, 38% of gate counts are reduced in reduced complexity SQRT CSLA than traditional SQRT CSLA adder circuits. Further, the performance of reduced complexity SQRT CSLA is compared with Compressor based adder circuits. Both compressors based digital adder and reduced complexity SQRT CSLA adder is incorporated into the addition part of Bi-Recoder multiplier independently. The performance of reduced complexity SQRT CSLA based Bi-Recoder is better than the performance of compressors adder based Bi-Recoder due to less hardware complexity of reduced complexity SQRT CSLA.

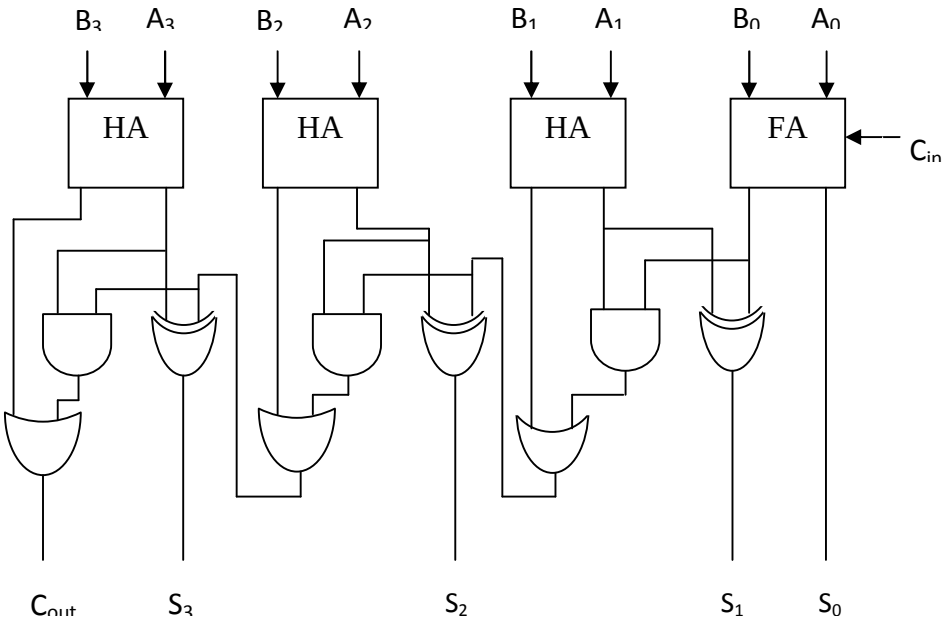

Figure 4: Architecture of 4-bit Reduced Complexity SQRT CSLA

Group Structures	Gate Count for Traditional BEC based SQRT CSLA	Gate Count for developed Reduced Complexity SQRT CSLA
Group-2	43	26
Group-3	61	39
Group-4	84	52
Group-5	107	65

Table 1: Gate Count of group structures of Traditional and Proposed SQRT CSLA

Both compressors based digital adder and reduced complexity SQRT CSLA adder is incorporated into the addition part of Bi-Recoder multiplier independently. The performance of reduced complexity SQRT CSLA based Bi-Recoder is better than the performance of compressors adder based Bi-Recoder due to less hardware complexity of reduced complexity SQRT CSLA.

4. DIRECT FORM FIR FILTER

Finite Impulse Response (FIR) filter is used to filter the noise/unwanted signals at finite impulse durations. Multiplication and Accumulation (MAC) unit estimates the duration of periodic impulses. Therefore, high performance of multiplication and accumulation architectures is required to improve the performance of digital FIR filter. In this paper, a novel, reduced complexity SQRT CSLA based Bi-Recoder multiplier is incorporated into multiplication of direct form FIR filter. Hence, absolutely we can improve the performance of digital FIR filter than other best existing FIR filters. The generalized structure of direct form FIR filter for N-taps is illustrated in fig. 5.

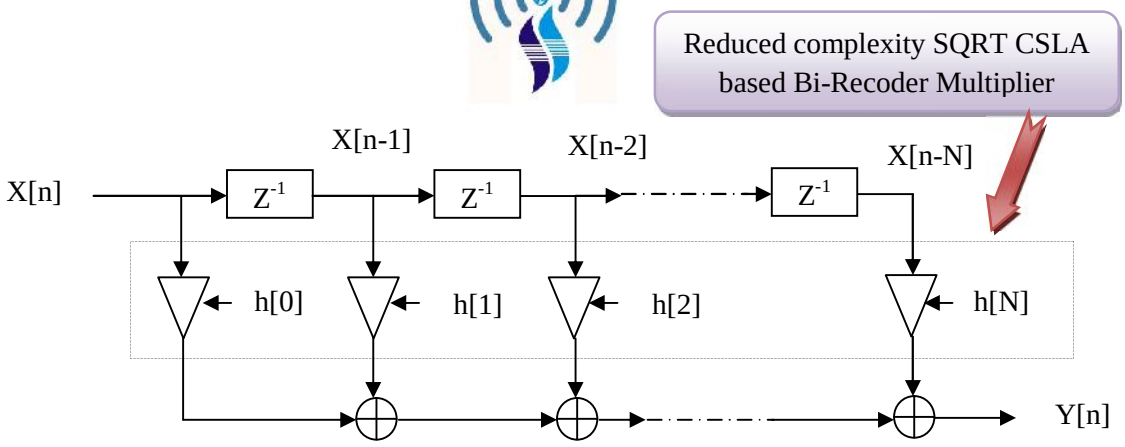

Figure 5: Structure of Direct Form FIR filter

This proposed work consider 3-tap FIR filter for 8-bit word length of input sample x[n]. Fixed coefficients also considered as 8-bit word length, which is indicated as h[0], h[1],..h[N] in fig. 5. The dotted line of fig. 5 indicates the incorporation of reduced complexity SQRT CSLA based Bi-Recoder multiplier into digital FIR filter.

5. RESULTS AND DISCUSSION

The aim of our proposal work is to increase the performance of digital FIR filter with

help of high performance MAC unit structures. To achieve our goal, a novel Bi-Recoder multiplier is designed by using Verilog Hardware Description Language (Verilog HDL). The developed multiplier reduces the hardware complexity than traditional multipliers. However, based on performance of adder structure only, we decide the best performance of multiplier. In order to fulfil this requirement, reduced complexity SQRT CSLA adder is developed in this work. This adder provides better performance in terms of area and power than traditional adders like compressors based adder. Hence, reduced complexity SQRT CSLA is incorporated into novel Bi-Recoder multiplier to increase the performance in terms of all VLSI concerns like less hardware complexity, low power consumption and high speed. Further to make comparison, compressors based adder is also incorporated into Bi-Recoder multiplier. The performances of both Bi-Recoder multipliers are analyzed and compared in table 2. Further the comparisons are graphically illustrated in fig. 6.

Types	Delay(ns)	Slices	LUT	Power(mw)
Bi-Recoder Multiplier using Compressor	31.469	77	145	978
Bi-Recoder Multiplier using Reduced Complexity SQRT CSLA	19.955	72	130	685

Table 2: Comparison of Bi-Recoder Multiplier by using different types of adders

From table 3, it is clear that a novel reduced complexity SQRT CSLA based Bi-Recoder Multiplier offers 6.4% reduction in silicon area and 36.58% reduction in delay and 29.95% reduction of power consumption than compressors based Bi-Recoder Multiplier. Next to, Multiplier design, developed Bi-Recoder multiplier is incorporated into digital FIR filter to improve the performance of digital FIR filter. To make comparisons compressors based Bi-Recoder multiplier also incorporated into FIR filter. The performance of both FIR filters are compared in table 2 and performances are graphically illustrated in fig. 7.

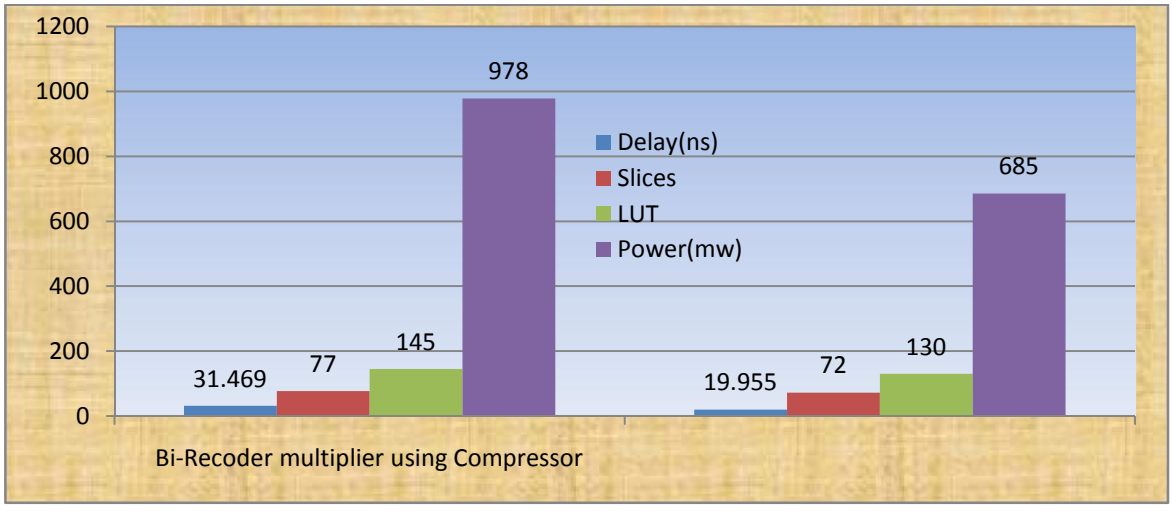

Figure 6: Performance of Bi-Recoder Multiplier by using different types of adder

From table 3, it is clear that proposed digital FIR filter offers 19.51% reduction in silicon area, 13.60% reduction in delay and 3.12% reduction in power consumption than existing digital FIR filter. Hence, a novel Bi-Recoder multiplier supports digital FIR filter absolutely to increase the performance of FIR filter.

Types	Delay(ns)	Slices	LUT	Power(mw)
Fir filter using Bi-Recoder Multiplier with Compressor	10.945	41	59	256
Fir filter using Bi-Recoder Multiplier with Reduced Complexity SQRT CSLA	9.456	33	48	248

Table 3 Comparison of FIR filter with developed and existing Bi-Recoder Multipliers

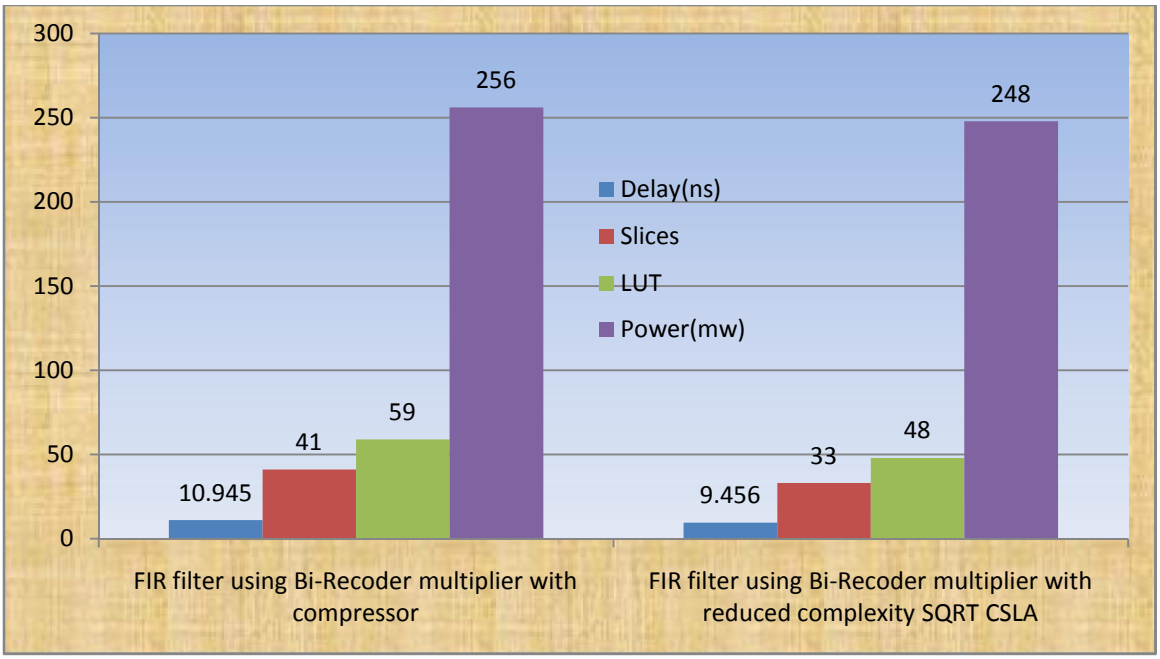

Figure 7: Performance of FIR filter with developed and existing Bi-Recoder Multiplier

CONCLUSION

In this paper, design of digital FIR filter is done by using Verilog Hardware Description Language (Verilog HDL). A novel Bi-Recoder Multiplier is introduced in this paper to increase the performance of MAC unit of digital FIR filter. Redundant logic functions of both traditional multipliers and adders are identified and removed in this work to increase the performance of MAC unit. Also reduced complexity SQRT CSLA is developed in this work, which is used in addition part of novel Bi-Recoder multiplier. Reduced complexity SQRT CSLA based Bi-Recoder Multiplier offers 6.4% reduction in silicon area and 36.58% reduction in delay and 29.95% reduction of power consumption than compressors based Bi-Recoder Multiplier. Further, developed and existing compressors based Bi-Recoder Multipliers are incorporated into digital FIR filter to compare the performances. The proposed FIR filter using Bi-Recoder Multiplier with reduced complexity SQRT CSLA offers 19.51% reduction

in silicon area, 13.60% reduction in delay and 3.12% reduction in power consumption than existing compressor based digital FIR filter. In future, the proposed FIR filter will be used to different types of signals, image and wireless communication applications and different types of signal processing techniques like Discrete Wavelet Transformation (DWT) and Discrete Cosine Transformation (DCT).

REFERENCES

[1] J. Chen, C. H. Chang, F. Fen., W. Ding, and J. Ding, "Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System", IEEE Transaction on Circuits and Systems, Vol. 62, Issue. 1, pp: 1-10, 2014.

[2] X. Lai, and Z. Lin, "Optimal Design of Constrained FIR Filters Without Phase Response Specifications", IEEE Transactions on signal processing, Vol. 62, Issue. 7, pp: 4532-4546, 2014.

[3] C. U. Kumar, and B. J. Rabi, "Area efficient FIR filter using graph based algorithm", In Current Trends in Engineering and Technology (ICCTET), 2nd International Conference on 2014, pp: pp. 495-498, IEEE.

[4] S. Patel, and B. Mohanty, "Area-Delay-Power Efficient Carry-Select Adder", IEEE Transactions on circuits and systems-II, Vol. 61, No. 6, pp: 418-422, 2014.

[5] R. S. Waters, and E. E. Swartzlander, "A reduced complexity Wallace multiplier reduction. Computers", IEEE Transactions on computers, Vol. 59, Issue. 8, pp: 1134-1137, 2010.

[6] V. Gowrishankar, D. Manoranjitham, and P. Jagadeesh, "Efficient FIR Filter Design Using Modified Carry Select Adder & Wallace Tree Multiplier" International Journal of Science, Engineering and Technology Research (IJSETR), Vol. 2, Issue. 3, pp: 703-711, 2013.

[7] A. P. Thakare, and S. Agrawal, "Design of High Efficiency Carry Select Adder Using SQRT Technique" International Journal of Emerging Technology and Advanced Engineering (IJETAE), Vol. 3, Issue. 7, pp: 97-100, 2013.

[8] B. Ramkumar, and M. K. Harish, "Low-Power and Area-Efficient Carry Select Adder" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 2, pp: 371-375, 2012.

[9] D. Paradhasaradhi, and M. Prashanthi, "Non-Linear Carry Select Adder Based Enhanced Wallace Tree Multiplier Structure", International Journal of Scientific & Engineering Research (IJSER), Vol. 5, Issue. 4, pp: 1361-1364, 2014.

[10] T. N. Priyatharshne, L. Raja,, and A. Vinodhini, "An Optimized Wallace Tree Multiplier using Parallel Prefix Han-Carlson Adder for DSP Processors" International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Vol. 3, Issue. 11, pp: 1700-1704, 2014.