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DESIGN OF LOW POWER 8T-XOR BASED 1 BIT-FULL ADDER USING CMOS

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ABSTRACT- This paper puts forward a methodology for designing 1 bit full adder using a 8T XOR. The 8T XOR is combined in a specific manner to get a full adder with sum and carry output. The resulting 1 bit full adder is made up of 22 transistors. The simulation is done using Tanner EDA (Electronic design automation) tool using 250nm technology and 5V power supply. The results show the efficiency of the parameters.

Keywords- [power; full adder circuit; transmission gate; NMOS; PMOS; MUX; XOR.]

1. INTRODUCTION

With the continuously increasing demand of laptops, portable personal communication systems and the evolution of shrinking technology, the research effort in low-power micro-electronics has been intensified and low-power VLSI systems have emerged high in demand. Digital integrated circuits commonly use CMOS circuits as building blocks. The continuing decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. In recent years, the growing demand for high-speed arithmetic units in CPU (central processing unit), ALU (Arithmetic logic unit), DSP (Digital signal processors) architectures and microprocessors has led to the development of high-speed adders as addition is an obligatory and indispensable function in these units. Adder is the core element of complex arithmetic circuits like addition, subtraction, multiplication, division, exponentiation etc. Thus, enhancing the performance of the full adder block leads to the enhancement of the overall system performance Ref. [1- 3]. As a result, design of a high performance full adder is very useful and important. Power dissipation has become Power dissipation has become a prime constraint in high performance applications, especially in portable and battery operated systems so it is necessary to reduce power consumption. With the development of CMOS technology, the minimum gate length of transistors continues to decrease, and the characteristic frequency also will be rising. With the lowering of threshold voltage in ultra deep submicron technology, lowering the supply voltage appears to be the most eminent means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles Ref. [4]. The Tanner EDA Tool is used for back-end designing and the S-Edit and T-spice tools for realizing the designed VLSI adders. The S-edit is used for designing of the schematic of a circuit

and T-spice is used to observe the output waveform on the W-edit screen.

2. DESIGN OF 1 BIT FULL ADDER USING 8T -XOR LOGIC (22T)

The XOR logic based 1-bit full adder cell has three inputs (X, Y, C_{in}) and two outputs (SUM, C_{out}). The fundamental relation between these three inputs and two outputs are shown in expression (1) and (2). XOR logic based 1-bit full adder can be partitioned into three elementary building modules. The first module is used for implementing Exclusive-OR between X and Y inputs and its complement. The second module computes SUM output using the outputs of the first module and input Cin while the module three is used to calculate the output carry (Cout) using the first module output and the Z, and input Cin. Fig.1. shows the relationship between the three modules. Structure of XOR logic based 1-bit full adder is shown in Fig. 1. It contains three modules (two XOR logic modules and a multiplexer). SUM and C_{out} signals of full adder cell being driven by the Y and Cin inputs. It can be seen that the output SUM is equal to the Z, when Cin= 0, and it is equal to Z when Cin= 1. Thus, a multiplexer can be used to obtain the respective value taking the Z input as the selection signal. Same as the above methodology, the output carry C_{out} is equal to Y when Z=0, and it is equal to Cin when Z=1. Z can be used to select the respective value for the needed condition, operating a multiplexer. Here XOR based 1-Bit Full-adder is realized with 22T as shown in Fig. 1 respectively. 22T full adders are realized with 8T transmission gate logic XOR modules respectively along with 6T multiplexer.

$$SUM = XYC_{in} + (X + Y + \overline{C_{in}})C_{out} \quad (1)$$

$$C_{out} = XY + (X + Y)C_{in} \quad (2)$$

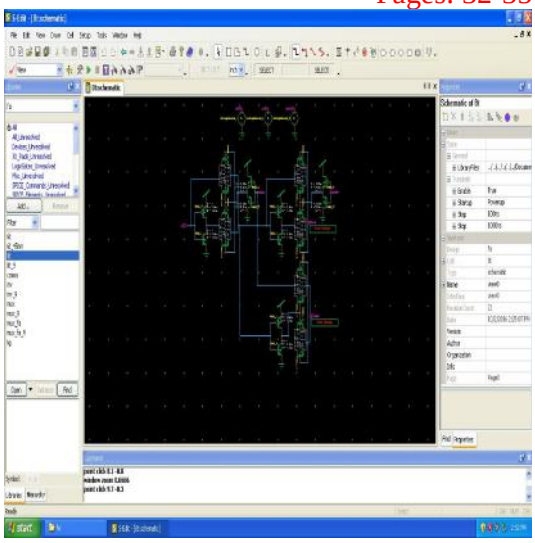

Figure.1. Design of 8T-XOR logic based 22T Full-Adder.

3. RESULTS

The proposed designs of 8T XOR based 1-bit full adder circuit with CMOS technology have been implemented by using Back End Tanner Electronic Design Automation (EDA) v14.1 tool. The output waveform for 8T XOR based 1-bit full adder circuit is shown in Fig.2. By using tanner, it will reduce the area and power consumption and also improves the performances of the full adder cells. The systhesis result for 8T XOR based 1-bit full adder is shown in Fig.3. The number of MOSFETS are 22, the number of voltage sources are 4, model definitions are 2, independent nodes are 13, total number of nodes are 18, MOSFET geometrics are 2, sub circuit instances are 0, computed models are 2 and the boundary nodes are 5. The synthesis result of power for 8T XOR based 1-bit full adder circuit is shown in Fig.5. The power value of 4-bit full adder circuit is 0.00977 watts. The output waveform of power for 1-bit full adder circuit is shown in Fig.4.

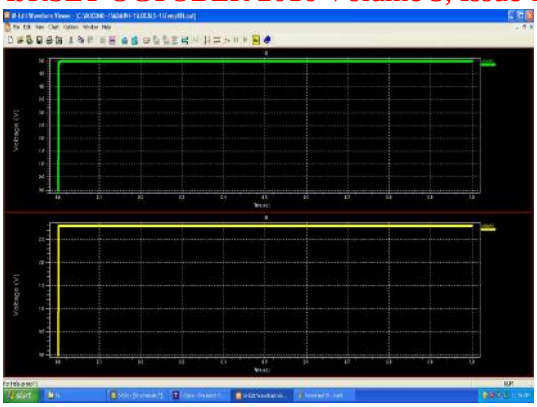

Figure.2. Output waveform for 8-T XOR logic based 22T Full adder.

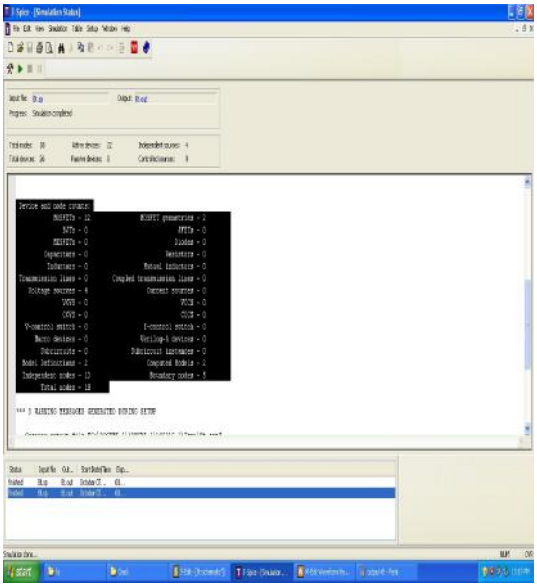

Figure.3. Sythesis result for 8-T XOR logic based 22T Full adder.

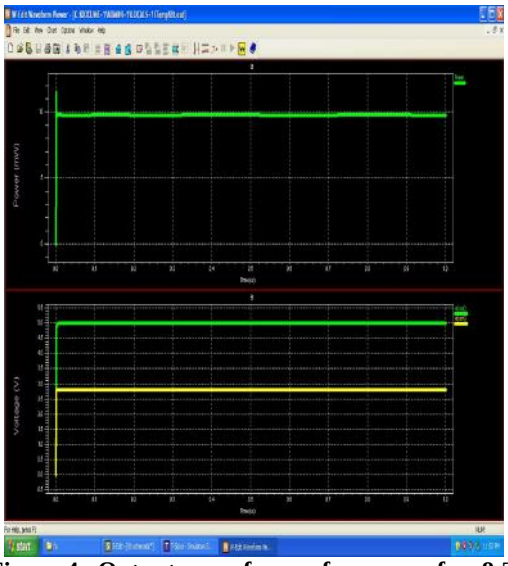

Figure.4. Output waveform of power for 8-T XOR logic based 22T Full adder.

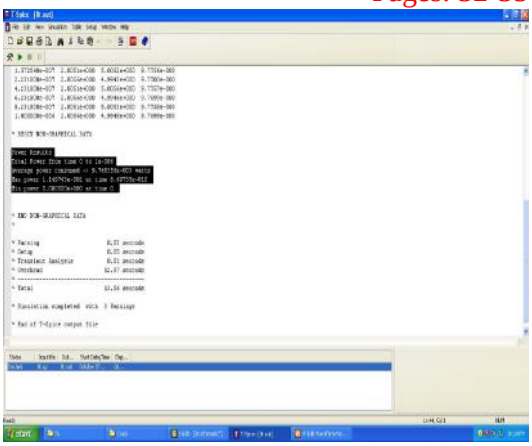

Figure.5. Sythesis result of power for 8-T XOR logic based 22T Full adder.

Adder configuration	Number of transistors	Power consumption
8-T XOR logic design	22	0.00977
6-T XOR logic design	18	0.0194
MUX based design	22	0.0104

TABLE I. Comparison of power consumption

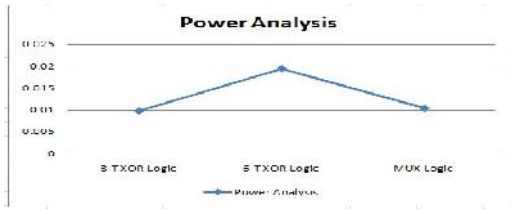

Figure. 6. Graphical representation of power consumption.

CONCLUSION

In this paper, 8T XOR based 1-bit full adder circuit is designed using tanner EDA tool through Very Large Scale Integration (VLSI) System design Environment. Less area utilization, high speed and lower power consumption are the important key factors in VLSI System design environment. The circuit was designed by using tanner EDA tool with CMOS technology and compared with other standard designs like 6T XOR, MUX based designs. The 8T XOR based 1-bit full adder circuit offers power value is 0.00977 watts .This full adder circuit is used to improve the overall performance of the structure.

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