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# DESIGN OF LOW POWER 4-BIT FULL ADDER CIRCUIT USING CMOS LOGIC

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**ABSTRACT-**This paper presents a performance analysis of hybrid 1-bit full-adder circuit design. The adder cell is dissected into smaller modules. The modules are analyzed and calculated extensively. To achieve a good-drivability, noise-robustness, and low-energy operations for deep sub micrometer to explore hybrid-CMOS style design. Hybrid-CMOS design style uses various CMOS logic style circuits to construct new full adders with desired performance .In this paper, a hybrid 1-bit full adder design employing both complementary metal oxide semiconductor (CMOS) logic and transmission gate logic is reported. In the proposed design of this paper first implemented for 1-bit full adder and then extended for 4 bit full adder circuit. The circuit was implemented by using Tanner EDA (Electronic design automation) tool. The 4 bit full adder circuit, which is used to improve the performance of the ALU operation. The proposed 4 bit full adder design is to enhance the speed of the operation and also reduces the area, latency and power consumption. The proposed 4-bit full adder circuit has energy efficient and outperforms several standard full adders without trading off driving capacity and reliability. The new 4-bit full-adder circuit successfully operates at low voltages. Performance parameters such as power consumption, delay and layout area were compared with the existing 1-bit full adder designs such as complementary pass-transistor logic, transmission gate adder and function-adder, hybrid pass-logic with static CMOS output drive full adder, and so on.

**Keywords -** [Complementary Metal-Oxide-Semiconductor (CMOS), Electronic Design Automation (EDA), Arithmetic and Logic Unit (ALU).]

## 1. INTRODUCTION

Adder is the most important critical building block in microprocessors and digital signal processors. In general, a 1-bit full adder core has three inputs and two outputs [1]. The increasing demand for low-power very large scale integration (VLSI) design can be focused at different design levels, such as the architectural, circuit, layout, and the process technology level [5]. At the circuits design level, considerable potential For power savings exists by means of correct choice of a logic style for implementing combinational circuits. The circuit logic style used in logic gates like speed, size, power consumption and the wiring net of a circuit. These designs have been broadly classified into two styles, static style and dynamic style.

Static full adders are more reliable, simpler with low power requirement but the on chip area requirement is usually larger compared

to dynamic full adder. The advantages of standard CMOS style based adders are strongest against voltage scaling and transistor sizing, while the disadvantages are high input capacitance and buffers [3]. Complementary pass transistor logic is not suitable for low-power applications. Several logic styles individually have been used to design simple and complex arithmetic circuits as flip-flops, XOR-XNOR cells, full adder cells, multipliers, dividers, etc. Classical circuits design normally use only one logic style for the whole circuit design.

The dynamic CMOS logic style gives a high speed of operation because the logic is built with only high mobility nMOS transistors. Due to the absence of the pMOS transistors, the input capacitance is also very low, and thus improves the speed of operation. However, it has several problems such as charge sharing and high clock load. The cmos logic style has high switching-activity and lower noise-immunity. It consumes the power in driving the clock lines. Dynamic logic style is more susceptible to leakage [2].

In the paper, proposed a new hybrid CMOS 4-bit full adder with driving capability .The full adder consists of pass transistor logic (PTL) and static CMOS logic is called as 'hybrid full adder'. A new three-input exclusive OR is first achieved, based on PTL operation,. The CMOS 0.35-µm process technology, the proposed 4-bit full adder is to have the minimum power consumption and less power, delay product by SPICE simulation.

## 2. DESIGN OF 4-BIT FULL ADDER CIRCUIT

The proposed 4-bit full adder circuit with CMOS technology is designed by using Tanner EDA tool. In this paper, 1-bit full adder is extended to 4-bit full adder. The proposed extended 4-bit full adder circuit, reduces the area, delay and power were compared with existing designs such as complementary pass-transistor logic, transmission gate adder, hybrid pass-logic with static CMOS output drive full adder. In the proposed structure, the numbers of transistor counts are decreased and also improve the overall performance of the circuit. In the proposed 4-bit full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit. This XNOR module is designed to minimize the power to the possible extend with avoiding the voltage degradation possibility. The single bit full adder cell designed for optimum performance may not perform well under deployment to real-time conditions. So the single bit adder cell is extended to 4-bit full adder cell to perform well in real time applications.

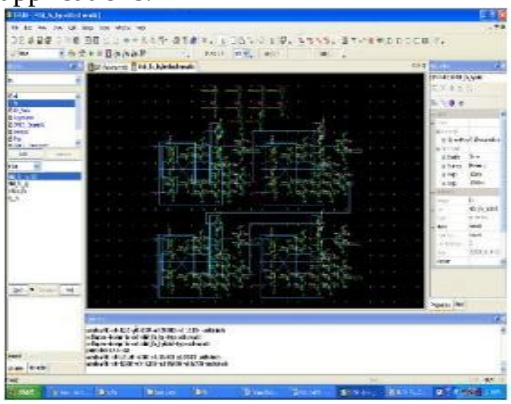

**Figure1- Design of four bit full adder circuit.**

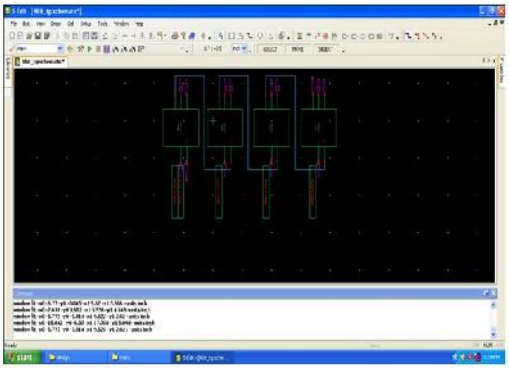

**Figure2- Schematic design of 4-bit full adder circuit.**

## 3. RESULTS AND DISCUSSION

The proposed designs of 4-bit full adder circuit with CMOS technology have been implemented by using Back End Tanner Electronic Design Automation (EDA) v14.1 tool. The schematic result of proposed 4-bit full adder circuit is shown in Fig.3. By using tanner, it will reduce the area and power consumption and also improves the performances of the full adder cells. The synthesis result of 4-bit full adder is shown

in Fig.4. The number of MOSFETS are 80, the number of voltage sources are 10, model definitions are 2, independent nodes are 32, total number of nodes are 43, MOSFET geometrics are 2, sub circuit instances are 4, computed models are 2 and the boundary nodes are 1. The synthesis result of power for 4-bit full adder circuit is shown in Fig.5. The power value of 4-bit full adder circuit is 0.01275 watts. The output waveform of power for 4-bit full adder circuit is shown in Fig.6.

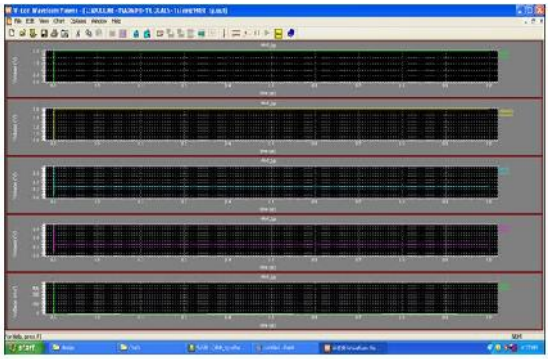

**Figure3- Schematic result of four bit full adder circuit.**

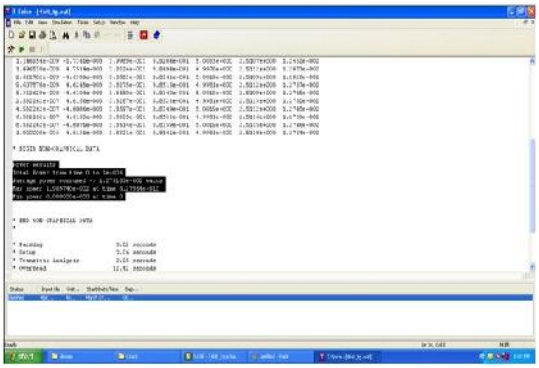

**Figure4- Synthesis result of proposed extended 4-bit full adder.**

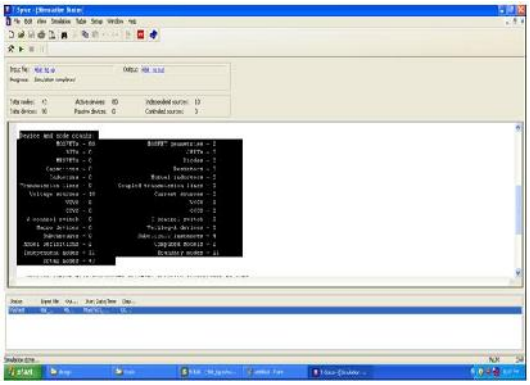

**Figure5- Systhesis result of power for 4 bit full adder circuit.**

| Cell name | Number of transistors | Area Analysis | Power analysis |
|---|---|---|---|
| Complementary pass transistor | 32 | 32 | 8.939 |
| Transmission gate full adder | 20 | 20 | 8.179 |
| Conventional full adder | 28 | 28 | 9.209 |
| Hybrid full adder | 20 | 20 | 2.190 |
| 4-bit full adder | 104 | 10 | 0.0125 |

**TABLE1- Comparison of power and area for various full adder circuits.**

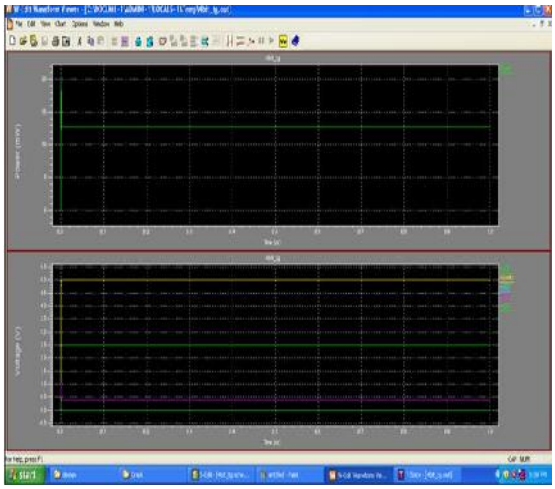

**Figure6- Output waveform of power for 4 bit full adder circuit.**

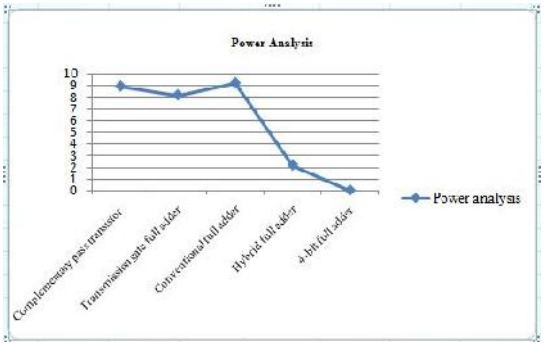


**Figure7- Graphical representation of power for full adder circuit.**

## CONCLUSION

In this paper, Extended 4-bit full adder circuit is designed using tanner EDA tool through Very Large Scale Integration (VLSI) System design Environment. Less area utilization, high speed and lower power consumption are the important key factors in VLSI System design environment. The circuit was designed by using tanner EDA tool with CMOS technology and compared with other standard designs like CMOS,

CPL, TFA, TGA and other hybrid designs. The extended 4-bit full adder circuit offers power value is 0.01275 watts .The proposed full adder was further used to implement 32-bit carry propagation adder having buffers at appropriate adder stages. When compared to single-bit Full adder, the proposed extended 4-bit full adder gives the better performances. This full adder circuit is used to improve the overall performance of the structure.

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