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DESIGN OF A 2.4 GHZ UP-CONVERSION GILBERT MIXER FEATURING CURRENT MIRROR TOPOLOGY AND CURRENT BLEEDING TECHNIQUE

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Abstract: -

In this paper, low voltage high gain up-conversion mixer, designed in 90nm CMOS technology, is proposed to work in the frequency band of 2.4 GHz. Current bleeding technique and current mirror topology are used in the upconversion mixer. Conversion Of an input of 100 MHz Given as intermediate frequency signal to an output of 2.4 GHz radio frequency signal is done by the proposed mixer with a local oscillator frequency signal of 2.3 GHz. Advantages of the proposed mixer are low voltage and high performance as compared with the conventional CMOS up-conversion mixer. At 2.4 GHz, the circuit has a conversion gain of 28.8db and a noise figure of 16db. This mixer works only at a low voltage of 1.2 V.

Keywords: - CMOS, high performance, up-conversion mixer, low voltage, current mirror, current bleeding

1. INTRODUCTION

Due to growing demand for wireless communications, it has led to increase in demand of low voltage and highly efficient circuits. In RF transmitter front-end, upconversion mixer plays a very important role as conversion of an incoming intermediate frequency signal to an output radio frequency signal is carried out by the mixer. Several different mixers have been proposed to meet the requirements in recent years. For direct conversion passive mixers have been adopted owing to their low flicker noise characteristics, but they have conversion loss[2]. Conventional gilbert mixer is generally used because of its advantages such as good port to port isolations.

This paper means to design a low voltage and high- performance up-conversion mixer for various WLAN transmitter applications [1].

2. OPERATIONAL PRINCIPLE

Based on the conventional and traditional gilbert-cell topology, a double balanced CMOS up-conversion mixer is designed. Current mirror topology [9],[10] and current bleeding technique[11-13] are used in both the driver and switching stages.

A. Current Mirror topology in the driver stage Due to non-linearity of the driver stage, the linearity of conventional gilbert cell mixer is not good. Since current mirror topology is highly linear, much better linearity can be obtained [14]. Therefore, current mirror comprising of M1-M3 and M4-M5 are added into driver stage having

degeneration resistor R1 connected between the outputs of the two current mirror transistors as shown in Fig. 1. Vb1 is used to provide constant trans-conductance over a wide selected range of input voltages providing high linearity.

The mismatch in the driver stage between the two current mirrors results in even-order distortion hence the degeneration register is used for linearization. The gain of the current mirror can be set by proper scaling of the current mirror transistors. It can be written as

$$K_{CM} = \frac{gm\ 3,5}{gm\ 2,6} = \frac{\left(\frac{w}{l}\right)3,5}{\left(\frac{w}{l}\right)2,6}$$

The conversion gain of the circuit can be increased by current mirror topology but the current mirror has a fundamental tradeoff between gain and bandwidth.

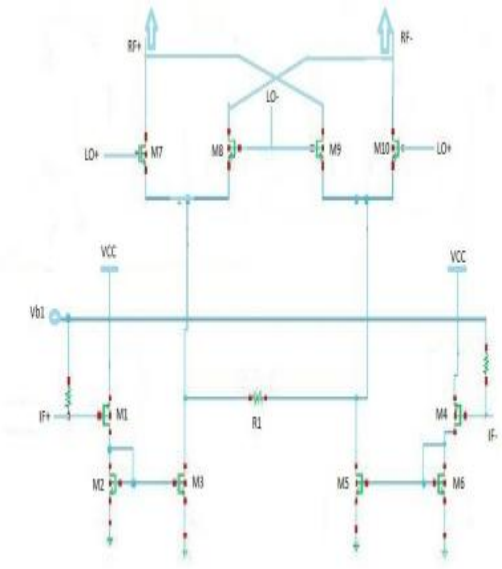

Figure. 1. Current mirror topology having a degenerative resistor in the driver stage.

B. Current Bleeding technology in the switching stage.

The current bleeding technique is the second improved method of the up-conversion mixer. Fig.2. Shows the bleeding circuit having two PMOS transistors (M11, M12) providing dc current into the driver stage. Due to the high output impedance provided by the PMOS pair which is in parallel with low impedance of the switching pair, the weak IF signal is made to go into the switching pairs, therefore with fast switching the gain of the mixer is maximized and also without increasing the current through switching transistors, the bias current flowing through the driver stage can be increased. Also, due to bleeding lower gate-source voltage is required for the switching transistors.

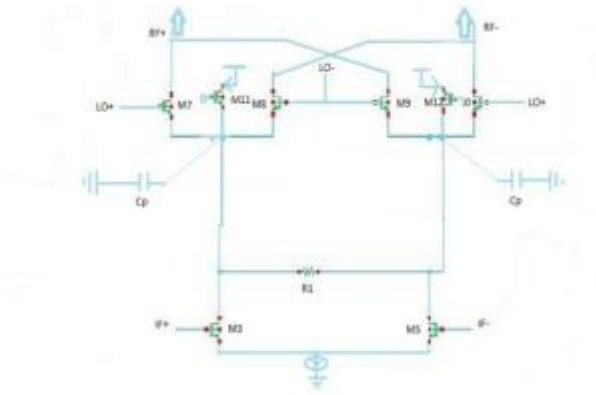

Figure. 2. Schematic of current bleeding with a degenerative resistor.

According to the Fig. 2. The tail capacitance of the LO switching stage is represented by the Cp. Thus, there will be a reduction in the conversion gain due to leakage of the IF signal to ground because of the tail capacitance Cp.

Therefore, our improved approach is to implement the current bleeding technique having an internal degeneration resistor R1 connected in between the common source node of the LO switches. The degeneration resistor will reduce the effect of Cp. As, this is an up-conversion mixer having the common source node of the LO switching working at low frequency, therefore, the LO leakage and current spikes are eliminated and also flicker noise is reduced and conversion gain is improved. The current bleeding topology having an internal degeneration resistor has good performance concerning conversion gain and noise figure.

3. CIRCUIT IMPLEMENTATION

Fig. 3. Shows the complete schematic of the proposed up conversion mixer consisting of several stages which include the IF input driver stage, the LO switching stage, current bleeding stage. Transistors M1-M3 and M4-M5 together constitutes the current mirror topology and act as the input driver stage. The received IF signals from voltage to current that formed the bias current of the upper four NMOS (M7M10) transistors can be transferred by the current mirror topology. The modulation of the current given by the driver stage is carried out by the upper transistors (M7M10) which will act as switching cores to modulate the current. The Transistors M7-M10 Are to be operated in the saturation region near the triode region so that they can work as ideal switches therefore, the current bleeding sources are used. PMOS transistors M11 and M12 are used to tune the bleeding circuit. To have high conversion gain and low flicker noise, a degeneration resistor R1 is used in the current bleeding technique and is adopted in the switching stage. On-chip capacitors, C1-C2 are applied as they will work as the DC blocking capacitors. Bias voltages refer to Vb1 to Vb4 having the maximum value at 1.2 V. Interference current signals can be ignored by means of resistors R2 to R9. Driving stage comprising of the current mirror topology and LO switching stage comprising of the current bleeding technique and use of a simple degeneration resistor in the driver and switching stage at the same time forms the main idea of the proposed up conversion mixer. The products other than the RF frequency at around 2.4 GHz are rejected by two parallel LC resonant Tanks (L1,C3) and (L2,C4) which will act as the band pass filters. Moreover, the signal at LO frequency in addition to the IF frequency are both mixed to the RF frequency. The design parameters of various instances in Fig. 3. Are summarized in Tab. 1.

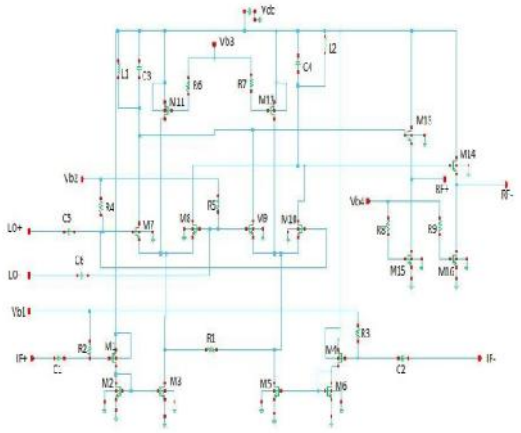

Figure. 3. Schematic of the proposed CMOS up conversion mixer.

Inst.	Para.	Inst.	Para.	Inst.	Para.
M1, M2	w/l=3/ 0.10um	C1, C2	6.6 pF	R1	10kΩ
M4, M6	w/l=3/ 0.10um	C3, C4	2.5 pF	R2, R3	20kΩ
M3, M5	w/l=30/ 0.10 um	C5, C6	6.8 pF	R4, R5	15kΩ
M7-M10	w/l=9/ 0.10um	L1, L2	3.39 nH	R6, R7	10kΩ
M11, M12	w/l=18/ 0.10um	M15, M16	w/l= 18/ 0.1 um	R8, R9	20kΩ
M13, M14	w/l=21/ 0.10um				

Table. 1. Summary of instance parameters.

4. RESULTS

The proposed upconversion mixer having the current mirror topology and current bleeding technique is designed in 90 nm technology and simulated using cadence virtuoso. In the layout, the arrangement has been placed as symmetrical as possible to minimize the mismatches. Extraction of the parasitic resistances and capacitances is also taken and considered and taken into account in the simulation. In this design, conversion of an input signal at 100 MHz to 2.4 GHz through a 2.3 GHz LO signal is carried out. The simulation results show that a large conversion gain can be obtained. The calculated noise figure of the mixer is 16db. Fig. 4.shows the transient analysis of the

upconversion mixer which shows the conversion of 100 MHz input signal to 2.4 GHz output signal through a 2.3 GHz LO signal. Fig. 5.shows the power dissipation of the circuit which is 22mw for 1.2 V power supply. The layout of the circuit having all the parasitic components is shown in Fig. 6.which occupies an area of 22700 um The specifications show that the proposed upconversion mixer achieves a high gain with good noise figure while converting a lo IF signal to a high RF signal.

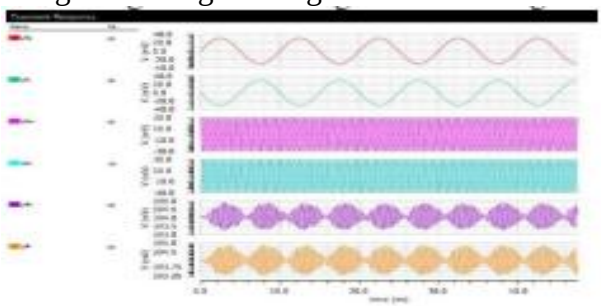

Figure. 4. Transient response of the up-conversion mixer

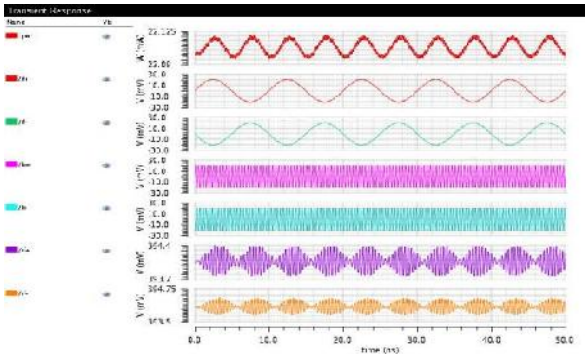

Figure. 5. Transient response with power dissipation

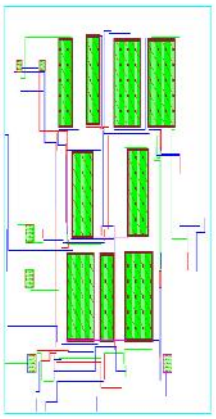

Figure. 6. Layout of the proposed upconversion mixer.

The specifications are summarized as below in Tab. 2.

CMOS Technology	90 nm
Power Supply	1.2 V
Area	22700um^2
IF Signal	100 MHz
LO Signal	2.3 GHz
RF signal	2.4 GHz
Conversion Gain	28.8db
Noise Figure	16db
Power Dissipation	22mW

Table. 2. Summary of circuit specifications.

CONCLUSIONS

This paper has presented the analysis and simulation of 2.4 GHz up-conversion mixer based on 90nm technology. Use of current mirror topology in the driver stage and current bleeding technique in the switching stage with a single degeneration resistor increases the overall conversion gain of the upconversion mixer. The proposed upconversion mixer has a large conversion gain of 28.8db and a low noise figure of 16db. The power consumption is 22mW from 1.2V supply voltage. The chip area of the proposed mixer is 22700um 2. This RF mixer is suitable for modern wireless communications owing to its low voltage and high-performance characteristics.

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