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DESIGN OF CMOS BASED FM QUADRATURE DEMODULATOR USING 45NM TECHNOLOGY

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Abstract:-

This paper presents the design of CMOS based FM Quadrature Demodulator for RF integrated circuits. This circuit is based on Bilotti's quadrature demodulator that uses a phase shift network, phase detector, and a low pass filter to filter out the high-frequency components. Phase shift network is an external RLC network. The Phase detector is implemented using Gilbert Cell and low pass filter using an operational amplifier. The power consumption of the circuit is 198uw with 1.2V supply.

Keywords: - Bilotti's Quadrature Demodulator, Gilbert Cell, Operational Amplifier, RF integrated Circuits

1.INTRODUCTION

DEMODULATION or detection involves changing the frequency variation in a signal into amplitude variations at baseband. Many circuits are used to demodulate FM. Some use discrete components while other uses integrated circuits.

FM detection can be realized using Slope detector, Ratio detector, Foster-Seeley detector, PLL detector, Quadrature Detector techniques depending on the design specifications requirements.

Slope detector converts the frequency variations into amplitude variations by using the slope of tuned circuit that can be detected by using a diode detector also called envelope detector. It can be used for both amplitude and frequency demodulation, so higher interference and noise will occur [11].

Ratio detector uses a double-tuned transformer to convert the frequency variation of input to amplitude variations. These variations are then rectified. It costs high as it uses a transformer and also not suitable for integrated circuit[12].

Foster-Seeley detector is same as ratio detector but with the difference that instead of third winding it uses the choke to ensure that no RF signal appears at the output. It is easy to construct as it uses discrete components, but expensive due to winding [11].

PLL detector works as a simple phase locked loop but with the difference that output is taken from loop filter and the voltage controlled oscillator is used in feedback. It can be incorporated into an integrated circuit easily, but it is not suitable for the design, where high linearity is required [11].

Quadrature detector is based on Bilotti's quadrature demodulator, which uses an external RLC phase shift network,

phase detector, and a low pass filter. It can be easily incorporated into integrated circuits. It is mainly used for high-frequency applications and the design where high linearity is required.[9].

2. PRINCIPLE OF DESIGN

In FM, If we assume s(t) to be sinusoidal signal then

$$s(t) = A_m \cos w_m(t)$$

Then the instantaneous phase deviation of the modulated signal is

$$\phi(t) = \frac{k_f A_m}{w_m} sinw_m t$$

The modulated signal, for the (FM signal) , is given by

$$S_m(t) = Acos(wt+\beta sinwt)$$

Where β the parameter is called the modulation index defined as

$$\beta = \frac{k_f A_m}{w_m}$$

The conventional method for design of demodulator integrated circuits is based on Bilotti's quadrature demodulator [4,5] that uses an external phase shift network to convert frequency deviation to phase, phase detector detect the phase and a low pass filter to avoid the high-frequency components at the output.

In this, we use Vin as the input voltage which is applied to one terminal of the phase detector. Another input of the phase detector is from the phase shift network. Phase shift network which includes an LC tank (L, Rp, Cp) and series capacitance shifts the input by a quadrature phase and provide it to the phase detector.

Gilbert cell double-balanced configuration based phase detector is used to detect the phase difference between two inputs. The phase detector compares the phase of the input signal to the signal generated by passing through a phase shift network and then it is passed to a low pass filter to get Vout.

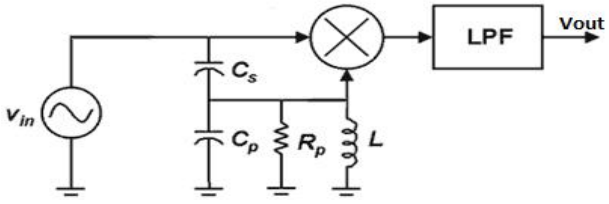

Figure.1. Block Diagram of quadrature Demodulator

Low-pass filter[13] consist of capacitance in parallel and resistance in series with the load. Reactance is exhibited by capacitance and resistance which blocks high-frequency signals which avoid their appearance at the load. At higher frequencies, the reactance will be dropped, and the capacitor will function as a short circuit. Low pass filter is implemented with the help of low pass filter.

The resonant frequency of the phase shift network is given as

$$w_n = \frac{1}{\sqrt{L(C_s+C_p)}} rad/s$$

$$f_r = \frac{1}{2\pi\sqrt{(C_s+C_p)}} (Hz)$$

Where C_s is series capacitance, C_p is parallel capacitance and L is inductance of the phase shift network.

3. FM QUADRATURE DEMODULATOR IN CMOS TECHNOLOGY

FM Quadrature demodulator using CMOS technology is implemented. In this, we designed the phase detector using Gilbert cell and low pass filter using the operational amplifier. Phase shift network is external RLC network. The transfer function of the RLC network is given as

$$H(s) = \frac{(C_s/2)L_p s^2}{(C_p+C_s/2)L_p s^2+(L_p/R_p)s+1}$$

Also, the center frequency and quality factor are given as

$$w_o = \frac{1}{\sqrt{L_p(C_p+C_s/2)}}$$

$$Q = R_p\sqrt{\frac{C_p+C_s/2}{L_p}}$$

The Gilbert cell mixer is a form of double balanced mixer that is a symmetrical topology to remove the unwanted radio frequency signals and local oscillator output signals from the IF by the cancellation. Double balanced Gilbert cell [1-3] based phase detector consisting of six NMOS transistors and a load

resistance through which output is taken. IF signal is the modulated signal to be applied and LO is the local oscillator signal. The output is linearly proportional to the difference of the phase of two input signals. In this linearity is improved as half of signal is processed by each side.

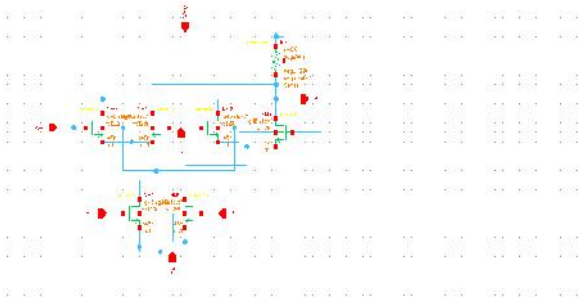

Figure.2 Double balanced Gilbert Cell

Operational Amplifier is designed using MOS. MOS are used instead of BJT MOS are smaller in size and dissipate less power. The Operational amplifier which provides single ended output by using differential input. Differential input is used to reject common mode signal.[1-3] The gain of the operational amplifier is 20 dB.

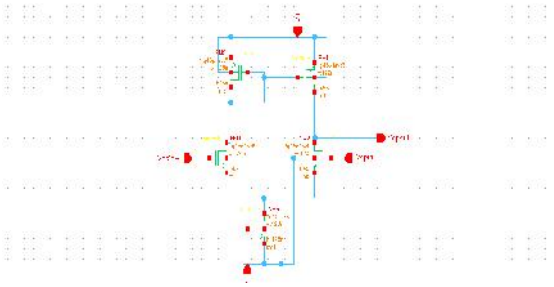

Figure. 3 Operational amplifier

A low pass filter passes signals with lower frequency and blocks that with higher frequency than the cut-off frequency. Low pass filter [8] circuit is designed using the operational amplifier. The Operational amplifier is used for filtering instead of RC network to improve the gain. The cutoff frequency of the circuit is given as

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

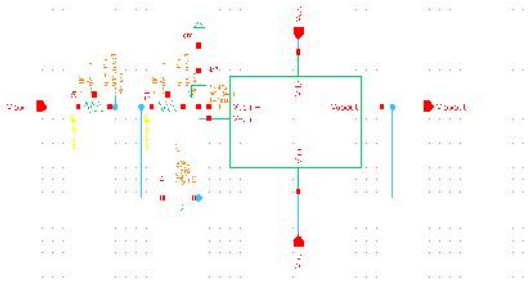

Figure. 4 Low pass filters

Quadrature FM demodulator based on the Bilotti's Quadrature Demodulator is implemented. It consists of phase shift network, a phase detector and low pass filter. The phase detector is implemented with the Gilbert cell. Phase shift network is implemented using RLC network. Low pass filter is implemented using the operational amplifier. In this, positive and negative inputs are applied to cancel common mode signals.

In this, we use an external phase shift network using an RLC network and two capacitances in series along with the positive and negative input.

Value for RLC network and series capacitances are

$Cs_1 = C_{s2}$ = 1p

R=10k, L=0.5 n, C= 6p

Input

Vquad = 0.5V , Frequency = 2.3GHz

Vdc= 1.2V, Vss= -1.2V,

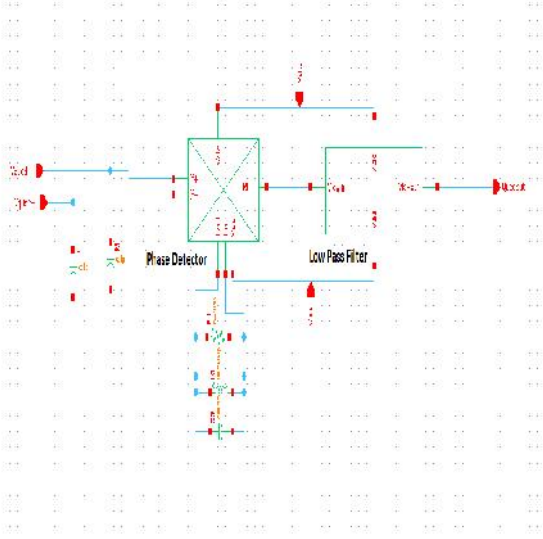

Figure. 5 FM Quadrature Demodulator

4. SIMULATION RESULTS

Transient Response of quadrature demodulator analyzed using cadence virtuoso simulator in 45nm technology with 1.2V supply voltage. The response shows the output of quadrature demodulator and the transient power consumed during operation.

Voltage conversion gain for the demodulator is calculated as the ratio of Vrms at the output to the Vrms at the input.

Vrms for the circuit at the input is **353mV** and Vrms at the output are **1.09V.**

Voltage conversion gain for Gain this demodulator is **9db**.

Power consumption for this demodulator is **198uW.**

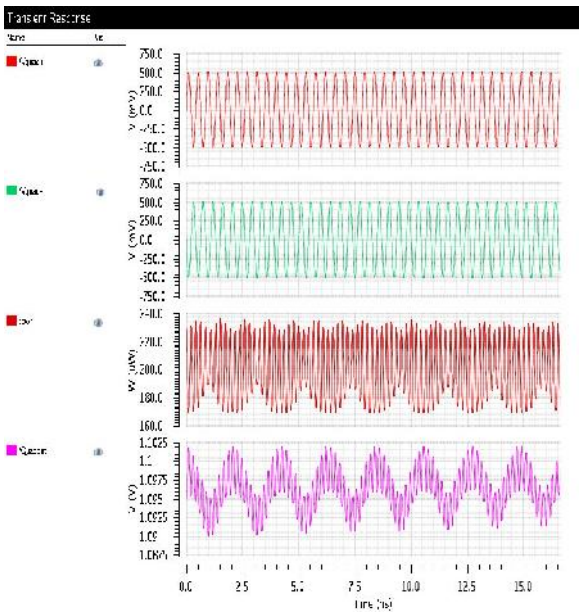

Figure.6 Transient Response of quadrature demodulator

5. LAYOUT FOR FM DEMODULATOR

The layout of the quadrature demodulator is shown below. The layout of the demodulator is realized using Cadence Virtuoso layout in 45nm technology.

In this layout of resistance is realized as **resnsdiff** and that of capacitance as **nmoscap1V** in GDPK 45 library of cadence virtuoso.

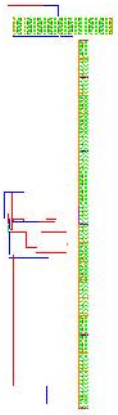

Figure.7. Layout of FM Quadrature Demodulator

The layout consists of the phase detector and low pass filter only. Phase shift network is not implemented in the layout as it consists of RLC network which will increase the layout area. Phase shift network is external to the demodulator.

The layout area of the demodulator is **28214.6231.**

CONCLUSION

In this paper, a CMOS implementation of a differential input FM quadrature demodulator has been presented. Due to large values of passive LC component, the LC tank circuit cannot be VLSI implemented. As a consequence, the circuit uses an external phase shift network, a differential input connected to assure a performing rejection of the common mode perturbations. The simulations performed in 45nm CMOS technology confirm the theoretical result.

This research's aim was to design an FM quadrature demodulator for receiving an FM audio signal with low power consumption.

In this paper, CMOS implementation of Quadrature demodulator in 45nm technology is presented. In this, we have used 1.2V supply voltage and frequency is 2.3 GHz.

The demodulator shown here can be improved by using an AND gate replacing the phase detector, which will work as a phase detector.

In this linearity may be affected as compared to this design which has high linearity.

FM demodulator can also be implemented using PLL which consists of the phase detector, low pass filter and VCO(Voltage Controlled oscillator). It can be easily implemented in CMOS as it not consists of passive components and also the layout area will be reduced. In this linearity will be average but external components will be reduced.

Parameters	This Design	5	9
Technology	45nm	0.18u	0.6u
Frequency	2.3G	10.7M	455k
Supply Voltage	1.2	3.3	2
Power	198u	NA	2.3m
Gain	9dB	NA	NA

Table for comparison with previous research.

External phase shift network is used in this circuit to reduce the layout area.

In this, we have used differential inputs to reject common mode perturbations.

In comparison to the previous paper, we have reduced supply voltage, channel length and also the power consumption.

This circuit can be used for high-frequency audio applications.

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