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DESIGN OF CMOS BASED FM MODULATOR USING 90NM TECHNOLOGY ON CADENCE VIRTUOSO TOOL

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Abstract:-

This work shows implementation of a radio frequency (RF) CMOS transmitter operating around 8 GHz, in a constant-envelope frequency - domain approach named Frequency Modulation in Ultra-Wideband (FM-UWB) and implemented using 90nM CMOS technology. Both the two main transmitter circuits are relaxation oscillator type blocks. The circuit is in ductorless; hence it is wideband tunable and saves large area. In this transmitter the triangular signal is also present that can be used advantageously. The control circuit helps to obtain an FSK oscillator which generates a triangular signal with two different oscillation frequencies. The D flip-flop power dissipation is 15.62 u W. It is controlled by the transmitted data. Also, by use of only MOS varactors, a VCO capable of achieving 1 GHz of tuning range bandwidth was implemented with the operating frequency around 8 GHz. VCO operating voltage 1 V with power consumption 12uW. In the implementation of the transmitter the basic blocks used are Buffer, D flip-flop, Relaxation oscillator for implementing VCO and carrier generation, and transmission gates. And at last, thelayout is also drawn using Cadence Virtuoso Tool in 90 nm technology. The area of layout implemented is 0.0716 mm^2 Simulations results are quite satisfactory. The circuit fulfills the desired goals of obtaining a low-power and low-cost transmitter, which is capable of achieving high data rates and uses already occupied RF transmission bands.

Keywords: - FM-UWB, CMOS Transmitter, Low-Cost, Low-Power, Low-Area.

1. INTRODUCTION

Nowadays we are surrounded by all kind of communication devices, the most common are televisions and radios, mobile phones and computers, and hence the fast access to information is now a basic demand.

From the past decade, due to the sudden growth of technological devices, short-range wireless networks management have become the major priority. The capability to share information between almost every devices created a need for RF bandwidths and high transmission data speeds.

Hence we require the development of compact circuits with least area and cost, with low power consumption and low voltage supply, leading to an increase of the research and study both in the semiconductors and communications industries and in academic environment. In the direction of short-range applications, Ultra-Wideband (UW) Radio Technology can have the potential solutions for many of the identical problems in the areas of radio systems engineering and spectrum management.

And the modern UWB approach is based on the optimally sharing of the already existing radio spectrum resources rather than searching for still available but possibly unsuitable new bands. This thesis aims the

implementation of a radio frequency CMOS transmitter/modulator using a 90nM CMOS technology based in a constant-envelope frequency-domain approach called Frequency Modulation in Ultra-Wideband (FM-UWB). The main key features are less area and cost, low power consumption and low voltage supply. FMUWB can be proposed as a standard for biomedical applications.

The transmitter implementation is based in two main blocks, a frequency-shift keying oscillator which is controlled by the data, and is the main element to generate a sub-carrier signal, and a (VCO) voltage controlled oscillator used to produce the carrier signal. Both the oscillators are inductorless giving less area and complexity to the transmitter , leading to a low-cost and a lowpower implementation.

2. PRINCIPLE OF DESIGN

The method of design of FMmodulator circuits is based on double FM scheme.First block is implemented using a low-modulation index called digital frequency-shift keying (FSK).

And the second block comprises of a high modulation index analog FM, thus producing a constant envelope signal having flat spectrum.

In this scheme the frequency shift keying oscillator (controlled by the data) is the main element to produce a sub-carrier signal.And the voltage controlled oscillator (VCO) is used to generate the carrier signal.

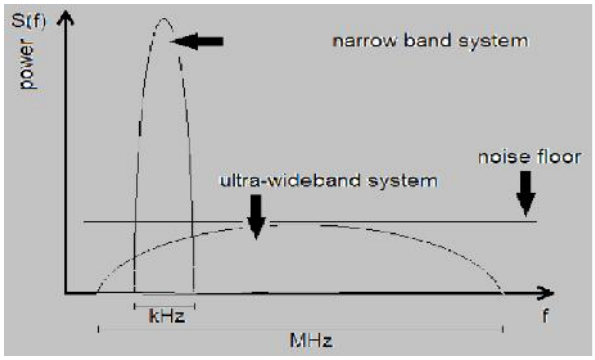


Figure.1. Narrow band & ultra-wideband system

In RF communication systems, modern ultra wideband (UWB) is used to describe the signals with a minimum bandwidth (BW) of 500 MHz (for operating frequency above 3.1 GHz)

3. FM MODULATOR IN CMOS TECHNOLOGY

The below circuit is implemented with ideal components for making this a high level circuit description. The circuit is the one of the best approach to validate the concepts involved in frequency modulation FM-UWB transmission technique.

All the circuits and simulations are developed and performed using the **Cadence virtuoso** tool.

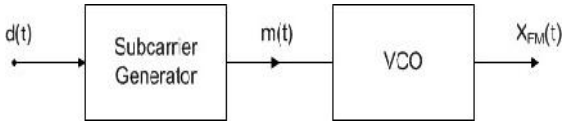


Figure 2. FM-UWB modulator block diagram.

The sub-carrier generator and the VCO (voltage controlled oscillator) both are implemented with the help of relaxation oscillator topology which can generate a sawtooth or triangular waveform.

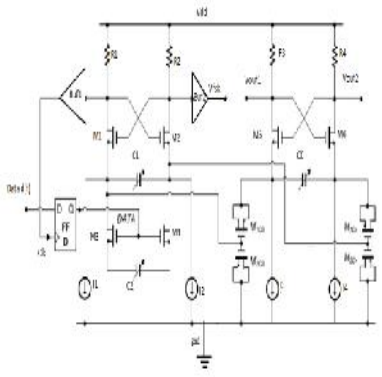


Figure. 3. Sub-carrier generator and vco implementation using relaxation oscillator

The data signal is a pulse waveform of high and low amplitude applied during transient analysis.

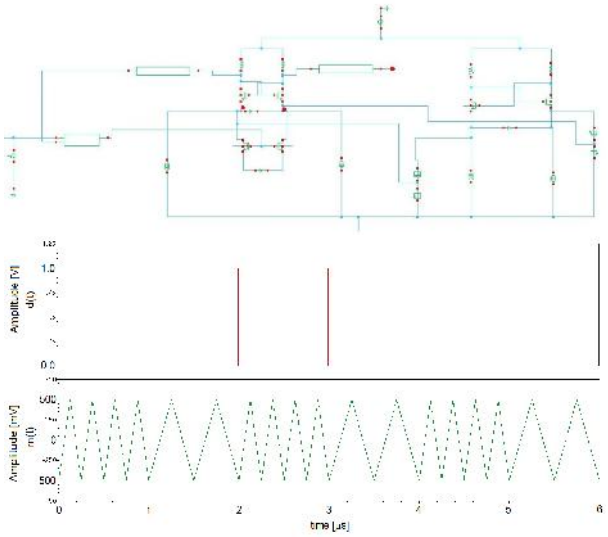


Figure. 4. FM Modulator implementation on cadence

3.1. Buffer

The buffer schematic is implemented by use of two cascaded inverters and applying the pulse waveform at the input of the circuit with vdd of the value of 1.8 v.Below given is the schematic of buffer and the output waveform of it.

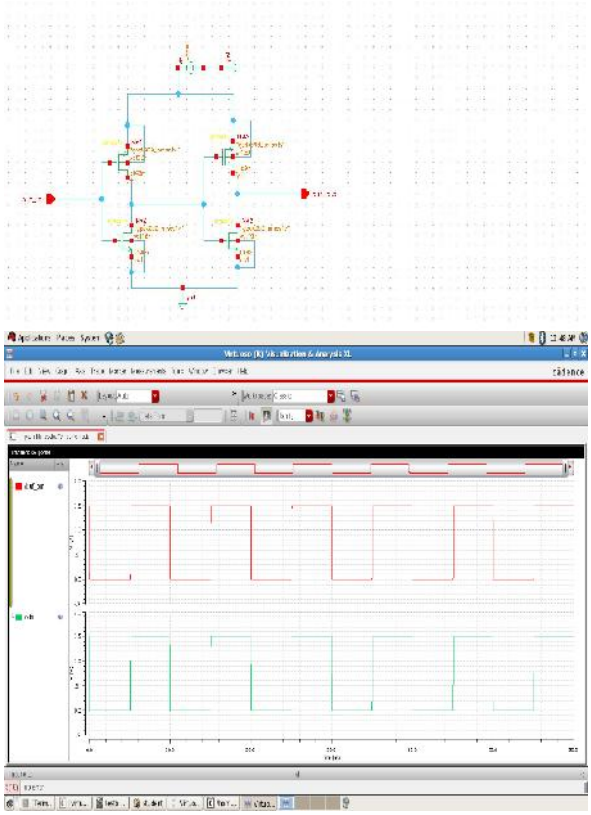


Figure. 5 Buffer schematic and output waveform

S. NO.	Component	No. of components	Value
1.	NMOS	2	W=120n,L=100n
2.	PMOS	2	W=120n,L=100n

Table 1 Components used in the buffer design

Buffer circuit is implemented by use of two inverters connected back to with each one Here in our main transmitter circuit, two buffers are used, one for the control logic whose output is used as the clock of the d flip flop.

Analysis of the Buffer

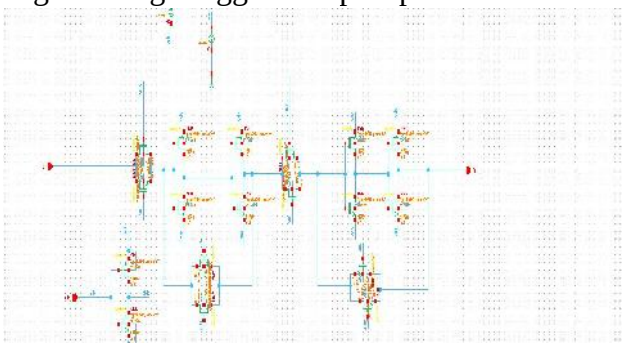
From the results simulated following analysis has ben obtained from the buffer Current consumption of 0.906 mA is achieved which will lead to high performance of the buffer as a component in the modulator design.

S. NO.	Parameter	Value
1.	Current consumption	0.906mA

Table 2 Analysis of the buffer

3.2. D Flip Flop

The D FF is used to delay the input waveform at the output. It is implemented by use of transmission gates with clk and inversion of clock. The D FF here is a negative edge triggered flip flop.



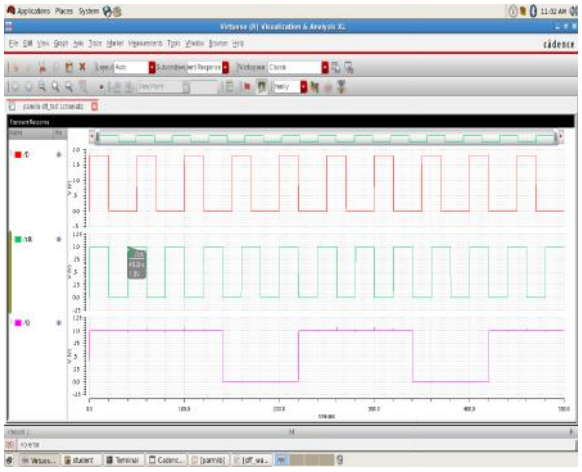


Figure. 6. D FF schematic and waveform

Analysis of the D Flip Flop

From the results simulated following analysis has ben obtained from the D Flip-flop Power dissipation is 15.62 uW is achieved which will lead to high performance D flip flop as a component in the modulator design.

S. NO.	Parameter	Value
1.	Power dissipation	15.62 uW

Table 3. Analysis of the D flip-flop

3.3. VCO implementation

The voltage controlled oscillator is the key element in a frequency modulation process, and one of the most challenging blocks to design.

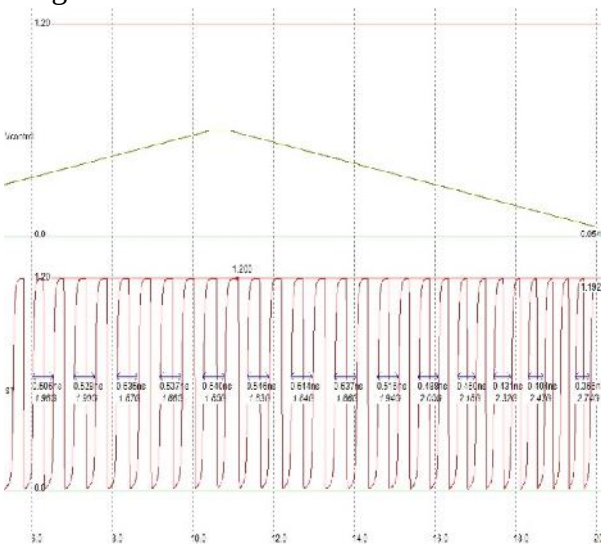


Figure. 7 VCO transient output

Parameter	VCO
Technology	90nm
Operating voltage	1V
Power Consumption	12uW

Table 4. Analysis of the VCO

4. SIMULATION RESULTS

Transient Response of modulator is analysed using cadence virtuoso simulator in 90 nm technology with 1.2 V supply voltage. The response shows output of modulator.

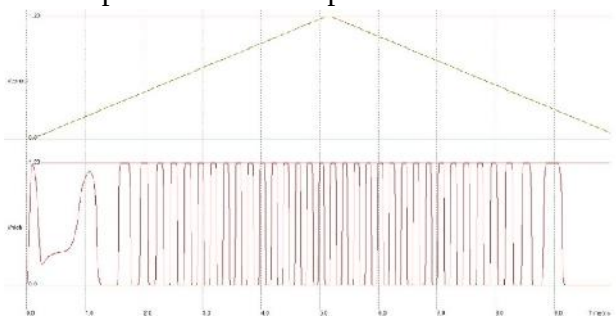


Figure.8. Transient Response of FM modulator

Block name	Output buffer	VCO	FSK oscillator
Current consumption	0.906 mA	6.092 mA	35.320 uA
Bandwidth	-	1.17 Ghz	-
Oscillation frequency	-	7.33 - 8.50 Ghz	2.16-4.42 MHz

Table 5. Analysis of the FM

The voltage difference between V_{tune1} and $V_{tune2}$is in the interval (**−240, 240**) **mV**, which means that v_C has an amplitude of about **480 mV**. The two $v_C$frequencies are 2.166 MHz **and** 4.442 MHz

The signal presents a frequency variation between **7.37 GHz** and **8.50 GHz** and its maximum and minimum voltage are **1.14 V** and **545 mV** respectively.

5. LAYOUT FOR FM MODULATOR

Layout for the FM Modulator is realized using cadence virtuoso 90 nm technology.

In this capacitance is realized as **nmoscap1v** and resistance as **resnsdiff** in 90 nm technology.Also all the components from analog library are replaced with pins.

5.1 Layout of VCO

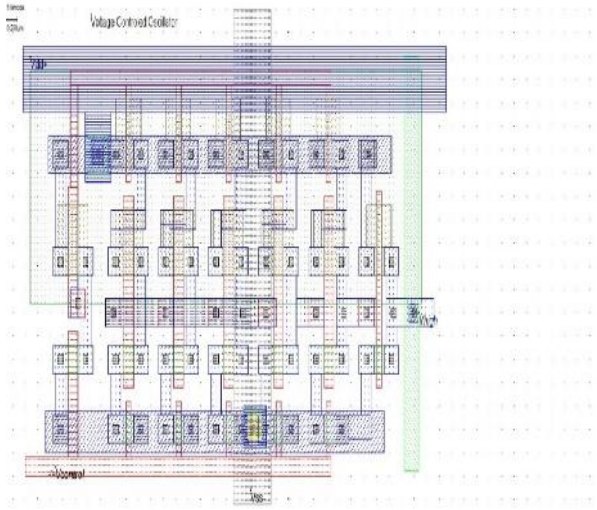


Figure. 9. Layout of VCO

5.2 Layout of FM modulator

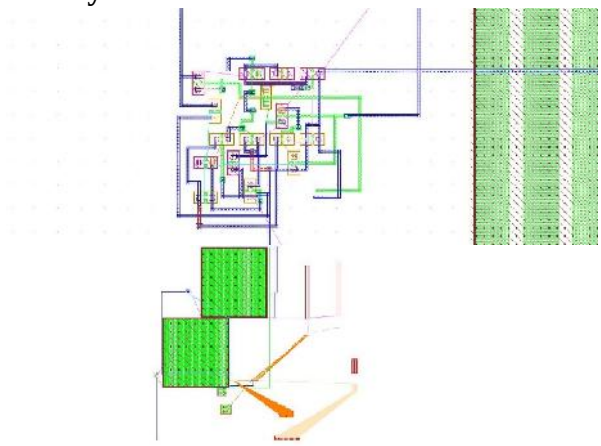


Figure.10. Layout of FM modulator

The layout shown above has an area of 351 mm x 202 mm ≈ 0.071 mm^2.

CONCLUSION

The main objective of this work was to implement a radio frequency (RF) CMOS transmitter operating around 8 GHz using a 90 nM CMOS technology. For that a study about Ultra-Wideband technology's basic concepts for adapting traditional narrowband frequency band into the modern Ultra-Wideband was performed.

A circuit topology was selected to fit the requirements. Inductorless circuit has to use for reducing the circuit area and leading to a price decrease. The approach was to use a relaxation oscillator topology which was based only on resistors and capacitors as passive elements, After circuit layout designing it is possible to conclude that there is a huge saving of area as compared with the circuits having inductors.

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